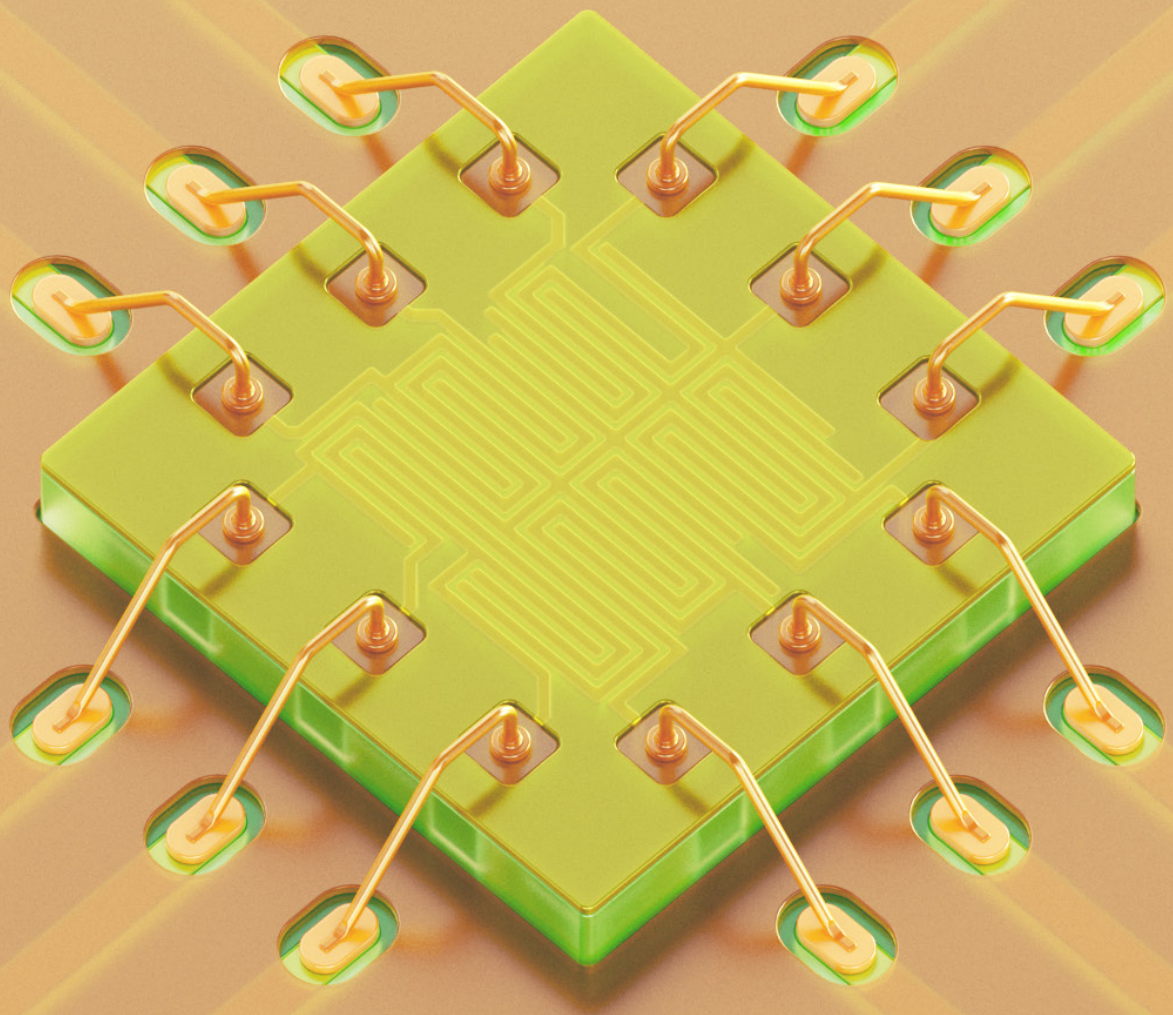
Altium

QUICK GUIDE

Wire Bonding

OCTOBER 2024



Wire Bonding Whitepaper

Executive Brief

Wire bonding is a crucial technology for establishing connections between semiconductor dies and circuit boards. It is a constantly advancing field, driven by the electronics industry's demands for miniaturization and compact design. Wire bonding can allow for higher performance and computing power to be achieved, enabling high-performance sensors and lighting, and unlocking the full potential of wide-bandgap semiconductors for high-power, high-density power conversion.

Possessing the appropriate PCB design tools and the expertise to accurately model wire bonds has become increasingly important. In this whitepaper, you will learn about the technology itself and how it can be used in a real-life design using Altium Designer. This proficiency will allow you to leverage the full potential of wire bonding and continually push the boundaries of innovation in electronics.

1. Introduction

Wire bonding technology remains the predominant method for first-level interconnections between semiconductor dies and the circuit board, accounting for over 75-80% of these connections in the microelectronics sector annually. The wire bonding equipment market, valued at approximately $800 million in 2022, is projected to surpass $1.6 billion by 2030, driven by the rising demand for increased computing power density, advanced packaging, and the adoption of wide-bandgap semiconductors [1].

For Chip-on-Board (COB) designs, where a semiconductor die is attached directly on a circuit board, wire bonding is preferred for its reliability, versatility, and cost-efficiency, offering a mature and established solution. Early widespread use of wire bonding COB can be seen in pocket calculators and electronic greeting cards. The significance of wire bonding is growing in addressing emerging electronics design challenges, such as increased processing power per area, highly integrated and dense LED arrays, image sensors, and high-temperature, high-power density electronics.

Deciding on whether to use chip-on-board versus a standard packaged chip depends on several factors such as board size and space constraints, performance requirements, customization and flexibility, manufacturing complexity and the level of effort required for development, and initial tooling costs.

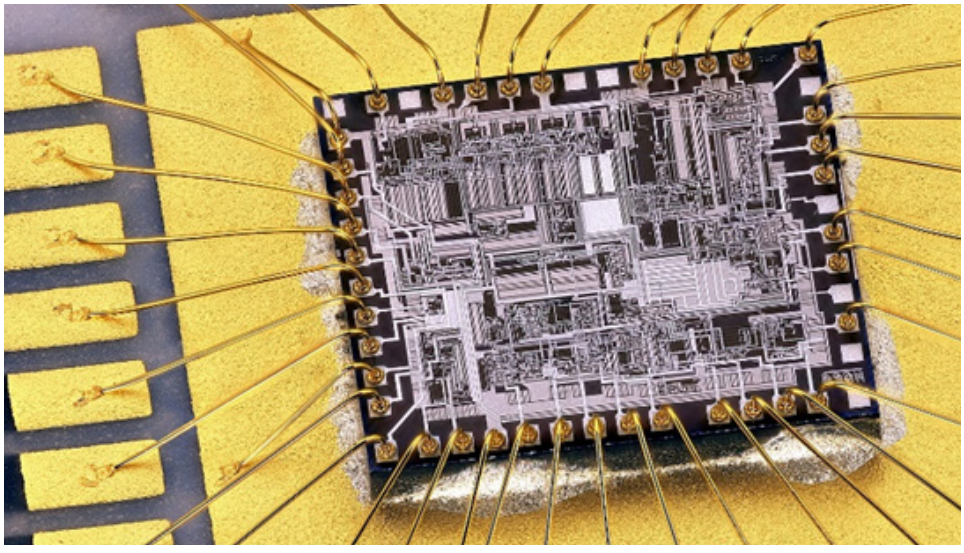


Figure 1. Example of wire bonding for chip-on-board (image source: Wikipedia)

2. Trends and Applications

Wire bonding is extensively utilized across the electronics industry, playing a crucial role in a variety of applications. It continuously evolves to meet the manufacturing challenges posed by emerging technologies. Notable areas where wire bonding is essential include advanced packaging, 3D integrated circuits, high-power LED modules, and power electronics. In these applications, wire bonding ensures reliable electrical connections, enhanced thermal management, and increased packing density. As new technologies and design concepts develop, wire bonding adapts to support higher performance standards, demonstrating its ongoing relevance and capability in the face of industry advancements.

3D Integrated Circuits

In today's advanced high-speed digital designs, bare dies are utilized to achieve high density and compactness. As the demand for increased processing power, memory, and I/O per unit area grows, design trends such as 3D stacking have emerged. Consequently, wire bonding technology has evolved and adapted to the fine pitch and high pin count requirements, making it the preferred, and often the only, method to address the challenges and complexities of interconnects in 3D die structures [2,3].

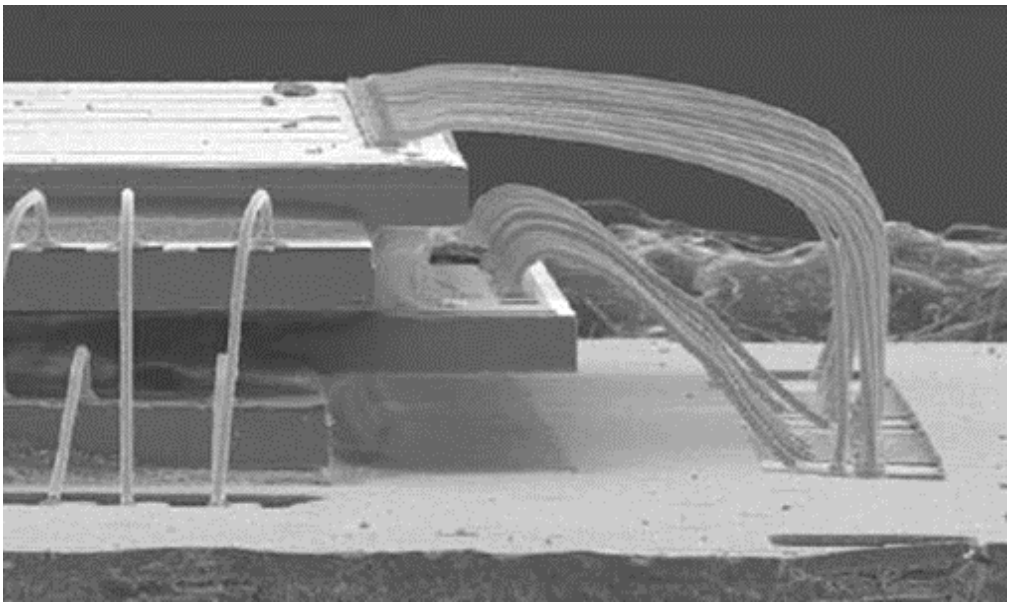


Figure 2. X-ray image showing stacked die with wire bonds [2]

Power Electronics - Wide-Bandgap Semiconductors

Power electronics have steadily evolved to meet the growing demand for renewable and clean energy, such as in electric vehicles and renewable energy generation. Wide bandgap semiconductors like silicon carbide (SiC) and gallium nitride (GaN) are crucial for achieving higher efficiency and power densities. The fast-switching speeds of SiC and GaN require meticulous PCB layout and routing, with close placement to DC links and decoupling capacitors to minimize power loops and reduce EMC issues [4]. Traditional die packages, such as TO-220 and TO-247, introduce parasitic inductances that impede the performance of SiC and GaN. Utilizing bare SiC and GaN dies, now available from manufacturers, allows for customized designs that maximize potential, enhancing power density and compactness. Wire bonding is essential for connecting these power dies in advanced applications, with heavy gauge copper wire bonding preferred for its ability to conduct higher currents at elevated operating temperatures.

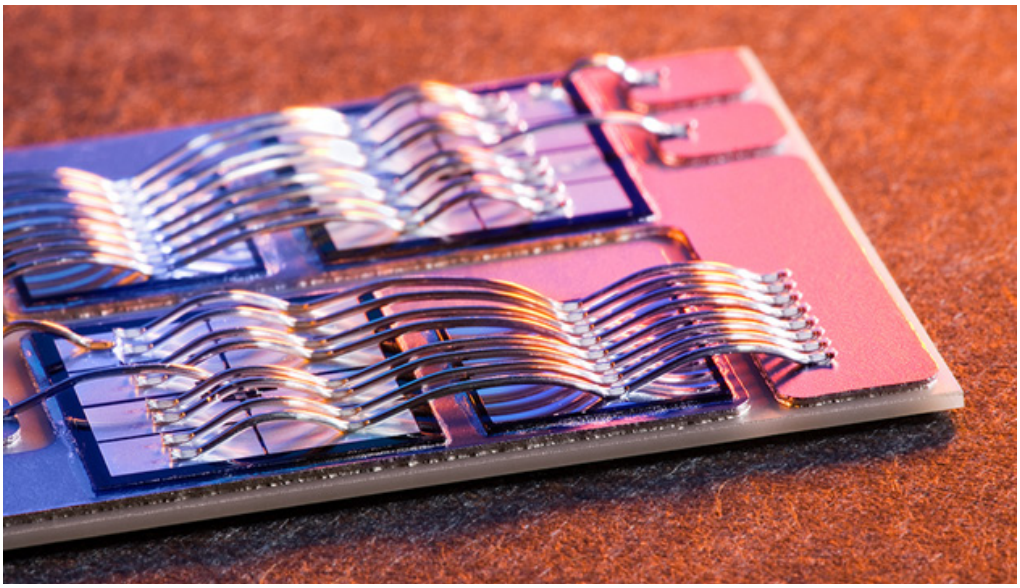


Figure 3. Wire bonded power module [4]

Optoelectronics - Image Sensors

Chip-on-board (COB) sensors, particularly in imaging applications, heavily rely on wire bonding. In these sensors, photodetectors and die pads are typically located on the same side (lateral construction), necessitating wire bonds to connect the die pads to the board or other nearby chips. New developments in high-resolution image sensors now contain hundreds of wire bonds spanning over a large area and have a 3D stack construction combined with processing cores. These developments are driving the need for finer pitch and smaller wire bond diameters. Consequently, wire bonding has now advanced to accommodate pad pitches as small as 35 um and wire diameters down to 0.6 mils [5], ensuring precise and reliable interconnections and facilitating the development of more compact and high-performance imaging sensors in various sectors such as consumer electronics, medical diagnostics, security and defense.

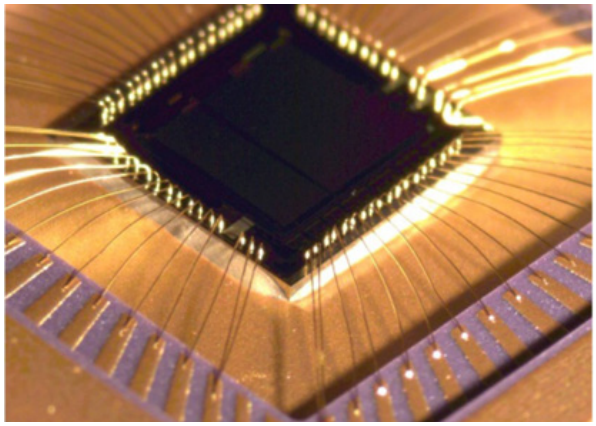


Figure 4. CMOS image sensor COB with wire bonds [image source: University of Alberta published in Sensors 2011]

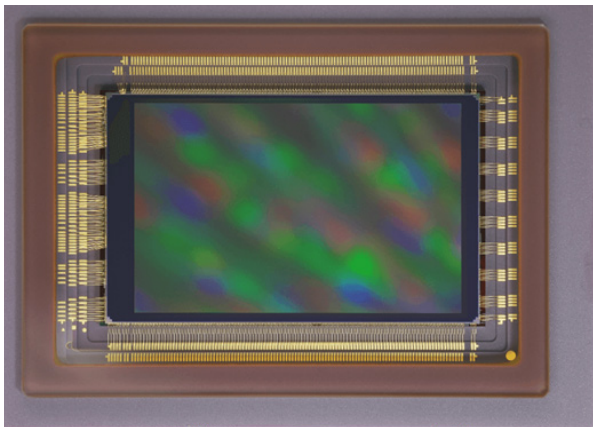


Figure 5. High-resolution CMOS image sensor with stacked bond wires (image source: Gpixel)

Chip-on-board LEDs

Mounting chip-on-board (COB) LEDs onto a substrate enables higher packing density and improved «lumen density» compared to packaged LEDs or flip-chip bonding. This results in more intense and uniform light with lower energy consumption and a smaller footprint. Wire bonding enhances thermal management, crucial for high-power LED applications, and allows for more compact designs, facilitating higher-density LED arrays and the miniaturization of lighting modules. By eliminating die packages and leads, electrical resistance is reduced, further improving the efficiency and reliability of LEDs. Gold wire bonding is preferred for COB LEDs, offering a cost-effective solution for low-volume production and enabling fine-pitch connections and chip-to-chip interconnections.

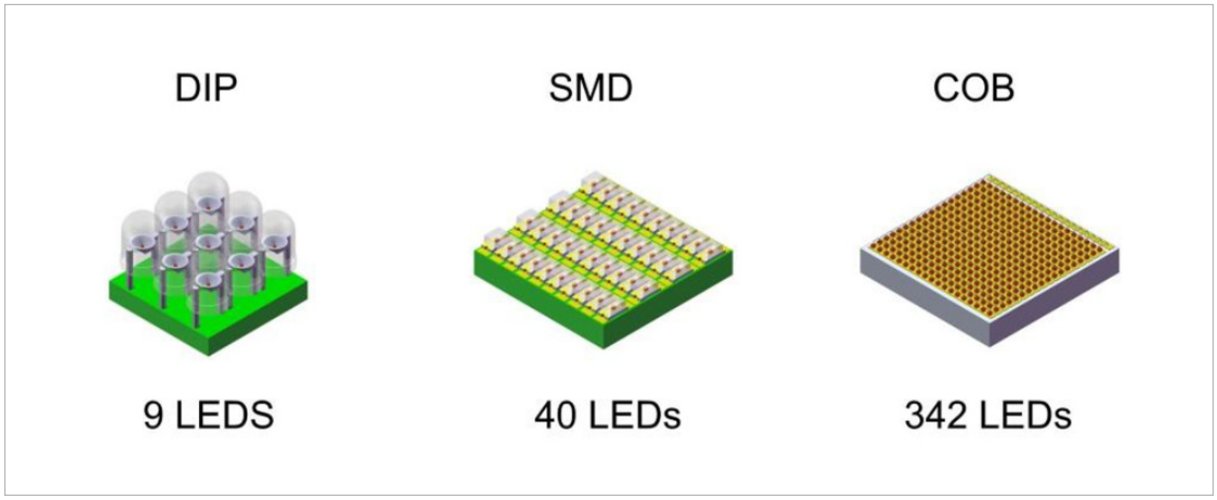


Figure 6. Comparison of LED array packaging (image source: Silicon Lightwords)

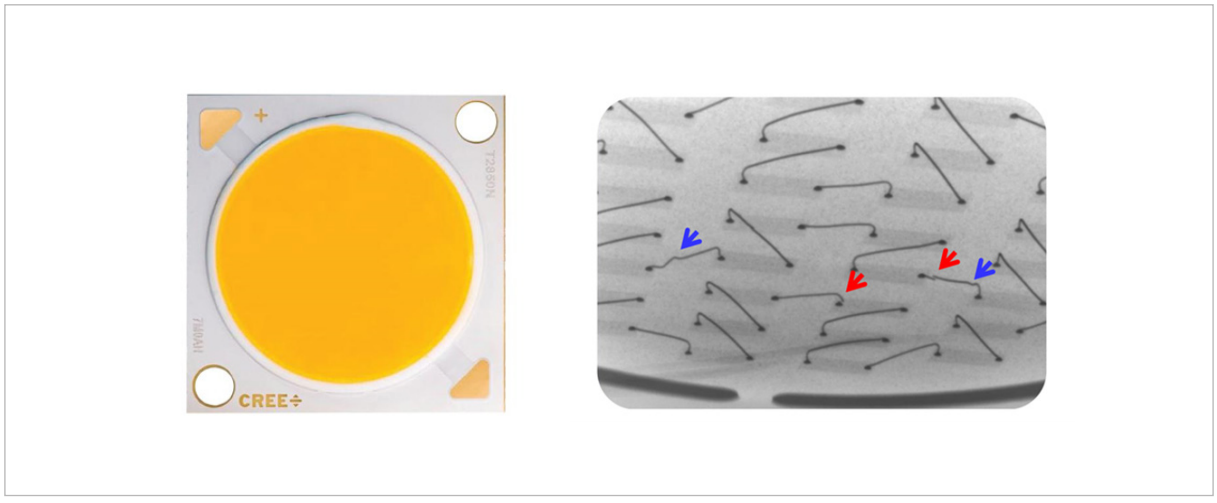


Figure 7. Example of COB LED array and x-ray image showing internal bond wires with signs of damage (image source: CREE)

3. Wire Bonding Costs and Considerations

Whilst the cost of using standard package chips is low for small to medium production volumes, COB can be more cost-effective for high-volume production at quantities in the hundreds of thousands to millions per year. This is because die packaging is eliminated, assembly costs could be lower too as there will be fewer unique components to assemble. COB designs allow for compact and densely packed designs that can have reduced size and weight, and hence less material. This can be seen in products such as pocket calculators, low-end multimeters and USB flash drives.

The cost of wire bonding itself varies significantly due to several factors including the materials used, application complexity, and production volume. Gold wire bonding is more expensive because of the high cost of gold, while copper and aluminum present more cost-effective alternatives. For example 0.8mil pure gold bonding wire can cost around $349/g whereas 0.8mil aluminum or copper bond wire can cost a fraction of that. The cost of a wire bonding machine and the necessary tools and infrastructure to support it can cost between tens of thousands dollars for manual and semi-automated machines to the hundreds of thousands for fully automated machines. For low-volume batches or non-recurring prototype COB designs it might be preferable to use an external manufacturer that provides a wire bonding service as that can be an intermediate cost-effective solution without the need to invest in wire bonding equipment and infrastructure. An external manufacturer can also guarantee better yields and a higher chance of a successful design.

Figure 8. A manual/semi-automated wire bonding machine for small-scale production and prototyping (image source: TPT Wire Bonder GmbH)

Figure 9. A fully automated wire bonding machine for high voltage production (image source: Hesse GmbH)(image source: Gpixel)

Contacting Manufacturers

When contacting a wire bonding service provider, it is important to be aware of the following which could impact the overall design and subsequently the cost:

- **Wire bonding material:** aluminum or copper wire bonding will be lower cost than gold
- **PCB surface finish:** for aluminum wire bonding ENEPIG surface finish is preferred, however ENIG and soft gold surface finishes can also be used. For gold wire bonding soft gold surface finish is preferred, ENEPIG can also be used
- **PCB manufacturing:** some wire bonding service providers can also build the PCBs, this can streamline the process and will be a faster overall solution. Alternatively, the PCBs could be built elsewhere and then sent to the wire bonding service provider. Ask for the maximum dimensions that the PCB could be and whether it should be penalized or not
- **Die attach:** some wire bonding services may not be able to attach the die on the PCB board, this may have to be done by you or another manufacturer. The die is typically attached to the PCB with an adhesive, this adhesive can be thermally and electrically conductive or not. Cost variations between the types of die attach is minimal.
- **Die sourcing and shipment:** the die itself can be either obtained by the wire bonding service provider directly from the die manufacturer or can be provided by you. Ask what die supply packaged is preferred. The most common die supply packaging is waffle pack, other types can be gel pack, tape on reel and even as a wafer.

Figure 10. Waffle pack (image source: TopLine Corporation)

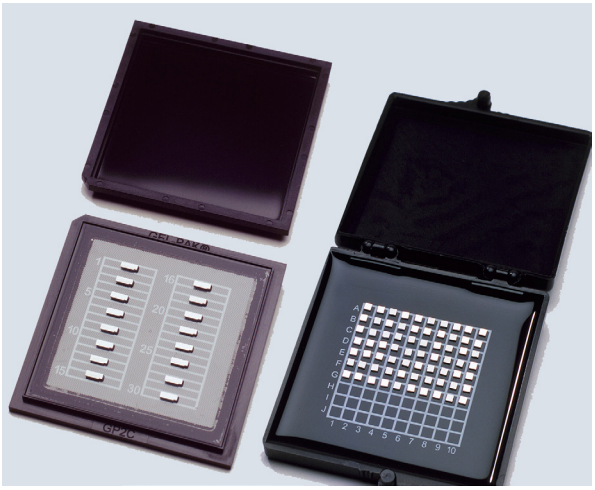


Figure 11. Gel pack (image source: Gel-box)

Cost Breakdown Example

As an example, we have the following COB design shown below. It has 21 wire bonds which will be aluminum wedge wire bonds, and we would like to get an initial estimate of the manufacturing costs for quantities up to 100. We've contacted several wire bonding service providers and PCB manufacturers to get an estimation of the overall cost breakdown, here we will share our findings.

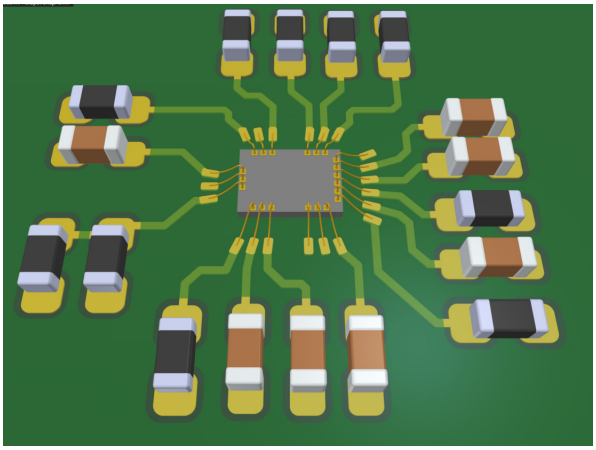


Figure 12. COB design example for cost analysis

For manufacturers and providers that use mainly automated or semi-automated processes for wire bonding the cost structure is similar to that of a standard PCBs, there are fixed tooling costs that do not change with quantity, and then there are costs relating to the number of units required. The cost per unit will decrease as the number of units produced increases. The cost breakdown below shows what can be expected from two manufacturers low volume semi- or fully-automated manufacturer

MANUFACTURER 1 (ASIA BASED)

Description	Cost for quantity of 25 (USD$)	Cost for quantity of 50 (USD$)	Cost for quantity of 100 (USD$)
Wire bonding service/tooling charge	500	500	500
Wire bonding process Aluminum wedge 1mil dia., 21 wires)	120	220	360
Bare die cost	125	120	115
Bare PCB with ENEPIG (6-layer, 0.8mm, 50×50mm)	557	582	590
Estimated Packaging & shipping	30	40	50
TOTAL	1332	1462	1615

MANUFACTURER 2 (EU BASED)

Description	Cost for quantity of 25 (USD$)	Cost for quantity of 50 (USD$)	Cost for quantity of 100 (USD$)
Wire bonding total cost (Aluminum wedge 1mil dia., 21 wires)	2460	3436	5370
Bare die cost	125	120	115
Bare PCB with ENEPIG (6-layer, 0.8mm, 50×50mm)	557	582	590
Estimated Packaging & shipping	30	40	50
TOTAL	3172	4178	6125

Other manufacturers that have a manual wire bonding process have a different cost structure where they might operate using a “day rate” cost. The cost breakdown below shows what can be expected from a manufacturer with a manual wire bonding process

Description	Cost for quantity of 25 (USD$)	Cost for quantity of 50 (USD$)	Cost for quantity of 100 (USD$)
Wire bonding process day rate (25 per day) (Aluminum wedge 1mil dia., 21 wires)	1600	3200	6400
Bare die cost	125	120	115
Bare PCB with ENEPIG (6-layer, 0.8mm, 50×50mm)	557	582	590
Estimated Packaging & shipping	30	40	50
TOTAL	2432	4162	7515

4. Reliability and Failures in Wire Bonding

Wire bonding is certainly a mature technology, and its failure modes and mechanisms are well understood which can be summarized as follows [6]:

- **Mechanical Failures:** Broken or lifted bonds due to improper bonding force or vibration, in addition to external forces from impacts, shocks and thermal expansions can lead to cracks and breaks along the bond wire.
- **Electrical Failures:** Poor electrical connections (high resistivity) from non-optimized bond parameters.
- **Thermal Failures:** Overheating and repeated thermal cycling can weaken the bonds or cause material degradation.
- **Corrosion:** Environmental factors causing oxidation or corrosion, particularly in copper wires.
- **Contamination:** Presence of foreign materials affecting bond integrity.
- **Bond Pad Cratering:** Excessive bonding force causing damage to the bond pad or underlying structures.

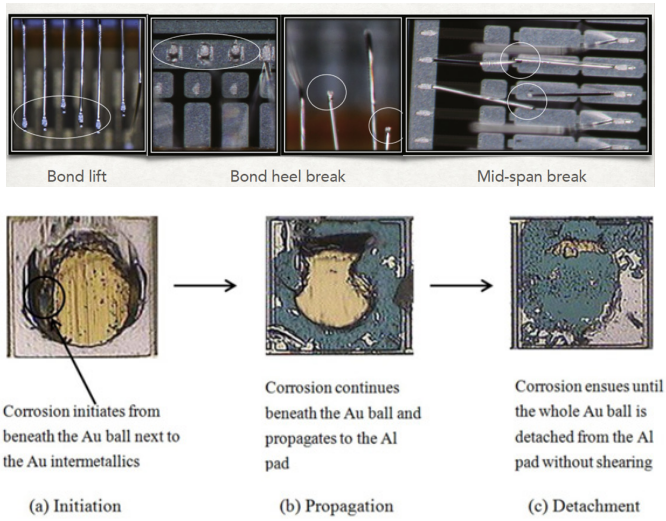


Figure 13. Images of different wire bond failure mechanisms [6]

5. Wire Bonding Design Tools & Specifications

The need for PCB design tools capable of modeling wire bonds is crucial as electronics designs become more sophisticated and compact. Making wire bonding technology accessible and incorporating it within PCB design software allows designers to accurately model and visualize wire bonds and enable them to predict and mitigate potential issues such as parasitic inductances, optimize component placement, and improve overall performance. Such a capability enhances the integration of bare dies, advanced packaging, and high-density interconnections, ultimately leading to higher quality and more efficient designs.

When designing for wire bonding, several aspects need to be taken into by the PCB design tool and the designer [7]:

- **Pad Design and Placement:** ensure proper pad size, shape, rotation and spacing to accommodate wire bonds without causing electrical shorts or mechanical failures.
- **Bond Wire Material:** choose appropriate materials for pads and wires (e.g., gold, copper, aluminum) based on conductivity, reliability, and cost.
- **Pad Surface Finish:** depending on the bond wire material it is recommended to have ENEPIG surface finish gold wire bonding, ENIG is recommended for aluminum wire bonding and ENEP is recommended for copper wire bonding.
- **Thermal Management:** design for efficient heat dissipation, particularly in high-power applications, to prevent bond degradation.
- **Mechanical Stability:** ensure that the substrate and bonding pads can withstand mechanical stresses during and after the bonding process.
- **Electrical Performance:** optimize for minimal parasitic inductances and resistances to maintain signal integrity and performance.
- **Protection:** it is recommended to add “glob top” to cover and protect the die and bond wires against environmental conditions such as humidity, temperature variations, and potential corrosive elements that may affect bond integrity over time. In LED and imaging applications lens holders can be used to provide both protection and light focusing.
- **Manufacturing Tolerances:** account for tolerances in the wire bonding process to ensure consistent quality and reliability in production.

By integrating these aspects into PCB design tools that support wire bonding, designers can create more advanced, reliable, and efficient electronic designs, pushing the boundaries of modern electronics innovation.

6. COB Wire Bonding in Altium Designer

Altium Designer’s new integrated Wire Bonding tool allows users to now create new hybrid design capabilities efficiently and accurately. Altium Designer integrated Wire Bonding tool has numerous benefits and features, some are described below:

- **Easy Validation of Bond Wiring in 3D View:** Visualize bond wiring, chip dies, and die pins alongside other parts of your project in Altium Designer’s 3D View. Wire bond diameter, height and die bond type can be configured with changes shown in 3D.
- **Ensure Design Integrity with Comprehensive Verification:** Designs rules and constraints can be defined for wire bonds to ensure all bonding connections meet stringent design requirements, preventing errors and maximizing yields. Automated DRCs verify bond wire to bond wire spacing, wire length, and connection integrity, providing reliable design outcomes.
- **Bond Wire Primitives and Layers:** Die pins and bond wires primitives are defined on new electrical layers outside the main layer stack to ensure clarity and accurate representation of wire bonding elements.
- **Wire Bonding at Library and PCB Doc Levels:** Dies and bond wires can be set up at both library and PCB document levels, unlike some competitor products that support wire bonding only at PCB level.
- **Versatile Bonding Options:** Connect various objects using wire bonding, including “Die to Bond Finger”, “Die-to-Die”, “Die to any Copper”, and “Copper to Copper”. This versatility allows for comprehensive and flexible design configurations to meet diverse project needs.
- **Support in Assembly and Documentation Outputs:** Generate assembly and documentation outputs that include wire bonding details. This support ensures that all necessary bonding information is accurately communicated to manufacturers, facilitating seamless production and assembly processes.
- **Advanced bond wire setups:** Support for Multiple Bond Wire Tiers, multiple Wires for the same die pin or bond finger, and bond finger alignment by wires.

7. COB Wire Bonding Design Example

7.1. Quick Start example

Once you have selected the appropriate wire bonding technology for your COB design, the PCB now must be set up to represent the COB in a way to meet PCB manufacturers' requirements for wire bonding, and also to ensure high yield rates and a successful operation of the design.

In this section we will have a look at how to set up wire bonding in Altium Designer for a COB design, and how to represent the bond wire connections which can then be included as a part of the PCB fabrication data. This is made possible by using a mechanical layer in the PCB to represent the die and the wire bonds.

The image below shows the COB wire bonding design example that we all aim to create. The design consists of COB with a few passive components connected to the wire bonding landing(finger) pads surrounding the COB. We will do that in eight steps as follows:

1. Footprint Creation & Importing Die Graphics
2. Wire Bonding "Data Layer"
3. Adding Wire Bonding "Landing/Finger Pads"
4. Drawing the Bond Wires
5. Pad Alignment and Orientation
6. Removing Solder Mask Along the Pads
7. Keep-outs and Courtyards
8. Generating Fabrication Data

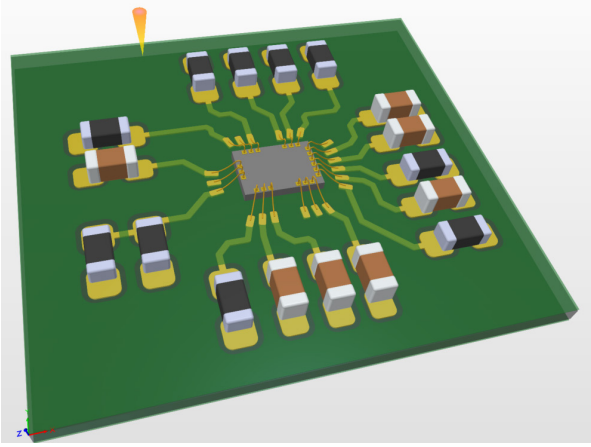


Figure 14. COB design example in Altium Designer

Using the new Wire Bonding Feature (AD2X)

> NOTE:
> Altium Designer 24.10 and above with a Standard subscription level are required.
> Wire bonding modeling and design feature is being developed for Altium Designer and is currently in Beta

STEP 1: Footprint creation & Importing die graphics.

First step is to create a die footprint which can then be used to create track connections to the rest of the circuitry. Similar to any other component, the footprint for the die can be added to an existing library that is either an integrated library or a project library. Alternatively a new library file can be created specifically for chip-on-board dies.

The footprint creation process begins first with the assumption that you have a CAD file for the die that includes the outline of the die body, its pads, and their locations. You can create the die and pad geometry outlines manually within Altium however it can be time consuming and complex especially for dies with a large number of pads.

The die in the image below will be used for this guide, its dimensions are 1770um x 1258um and has twenty one pads each with a dimension of 100um x 100um.

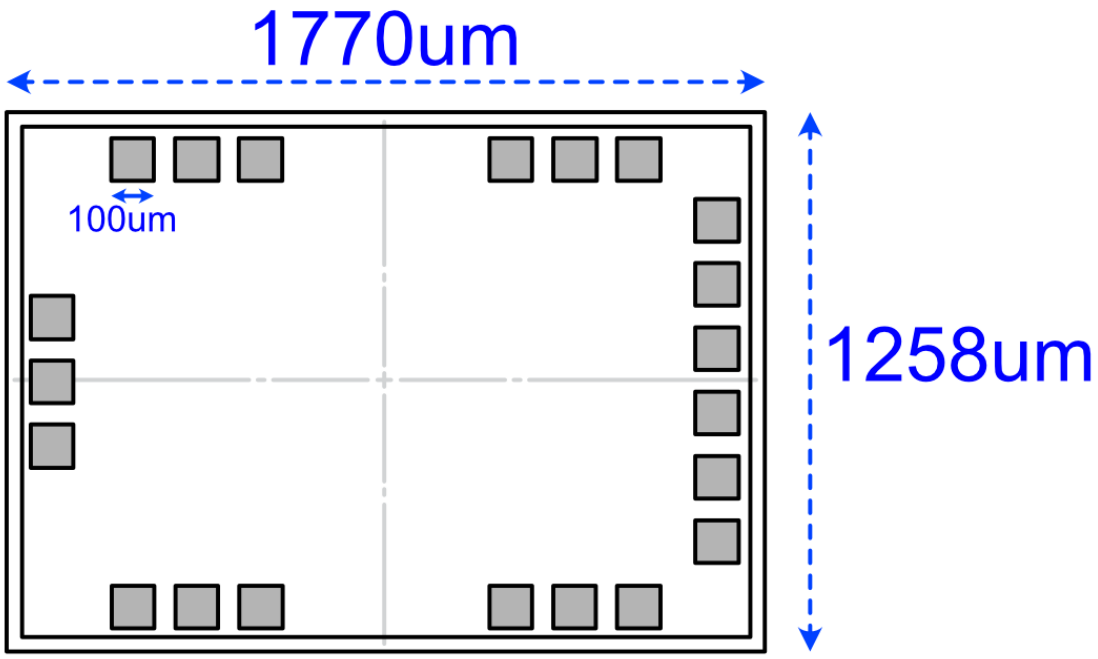


Figure 15. Bare Die drawing

Altium Designer can import CAD data which contains outlines of the die and its pads in the form of a DXF file. The DXF import settings allow you to choose the correct units, and on which layer to place the imported data. Once the import process is complete, it is recommended that the measuring tool is used to verify that the imported CAD data has the correct dimensions. The imported CAD data might need to be repositioned to be at the origin, and finally the imported data can be locked to prevent them from being modified or moved.

Note that Altium Designer's Wire Bonding tool can be directly used in a PCB document level (*.pcbdoc) for further editing and customisations. The additional example and use cases in the following sections will demonstrate how to achieve that.

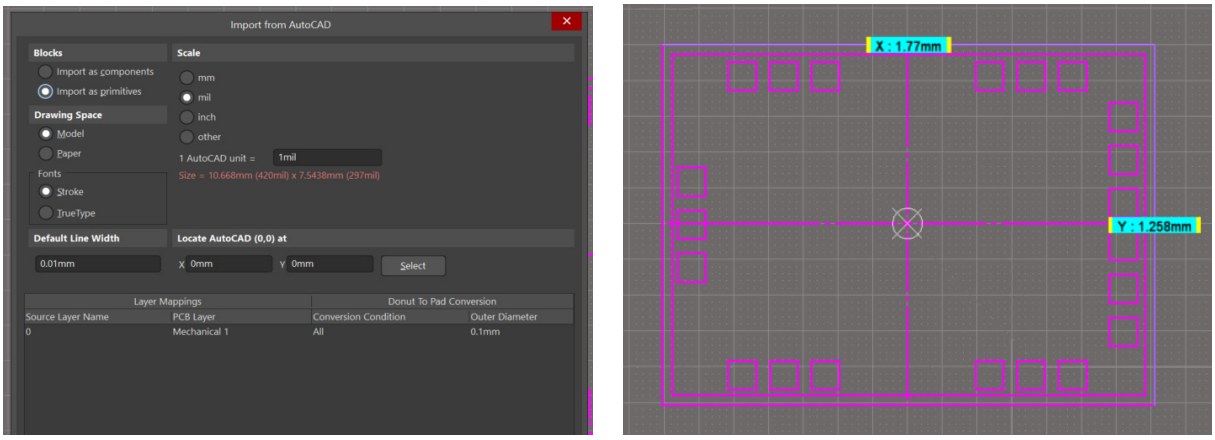


Figure 16. CAD data import

STEP 2: Wire bonding “Data Layers”

The new Wire Bonding capability in Altium Designer now introduces two “Component” layer pairs to represent the die and the wire bonds. These two new layers can be added as shown below

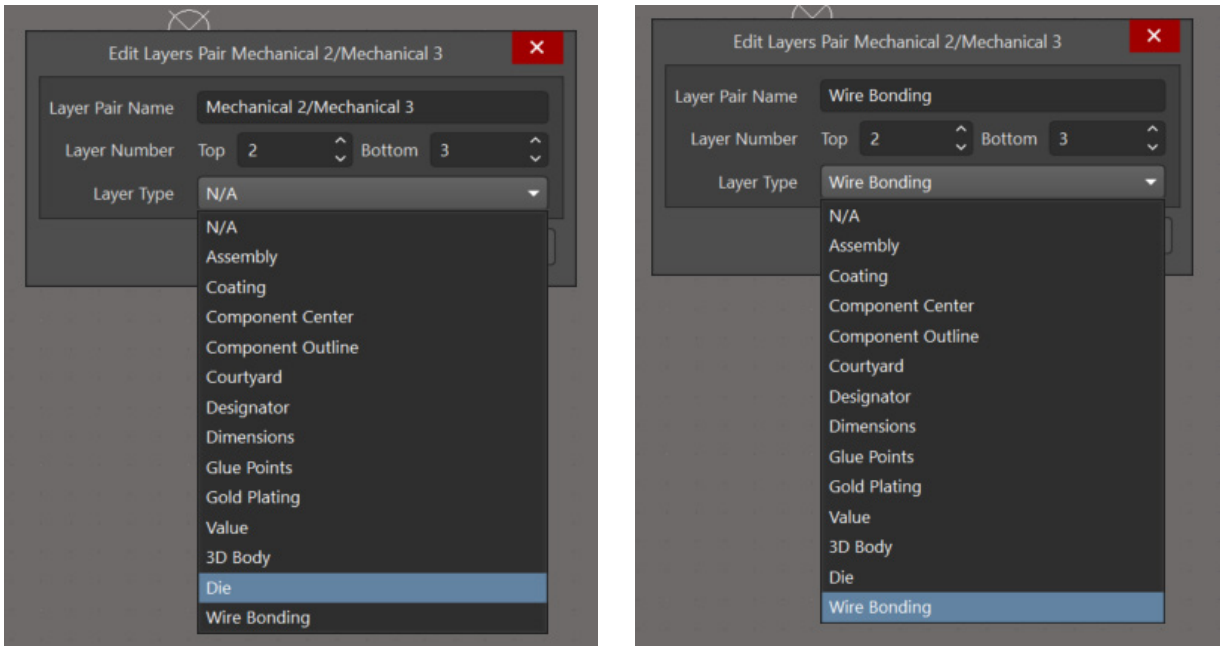


Figure 17. Die and wire bonding layers

Back to our imported (or created) die and pad data, we now need to assign those to the die and wire bonding layers. The die outline needs to be converted to a 3D body and placed on the Die Layer. The 3D body will be an extrusion whose height representing the die thickness can be controlled in the 3D body’s properties panel.

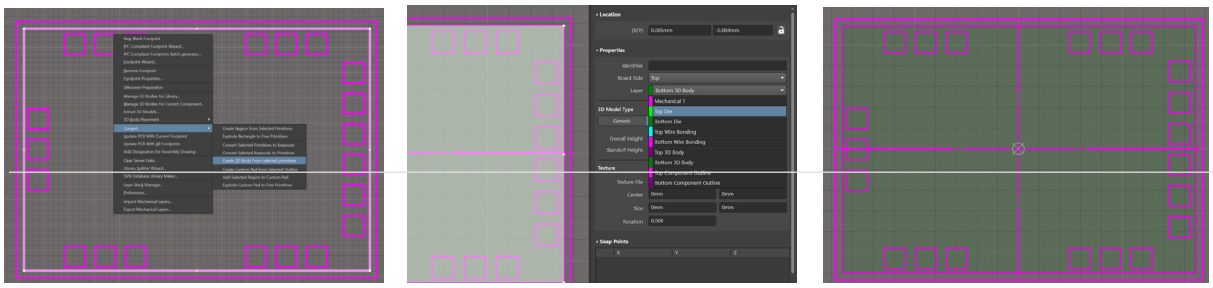


Figure 18. Die body creation and layer assignment

The outlines representing the die pads need to be converted to custom pad shapes and also moved to the Die layer. Altium will automatically know that these new pads belong to the die. Alternatively using the default pad primitives (Place → Pad) can also be used and must be placed on the 'die' layer of the needed bare die body.

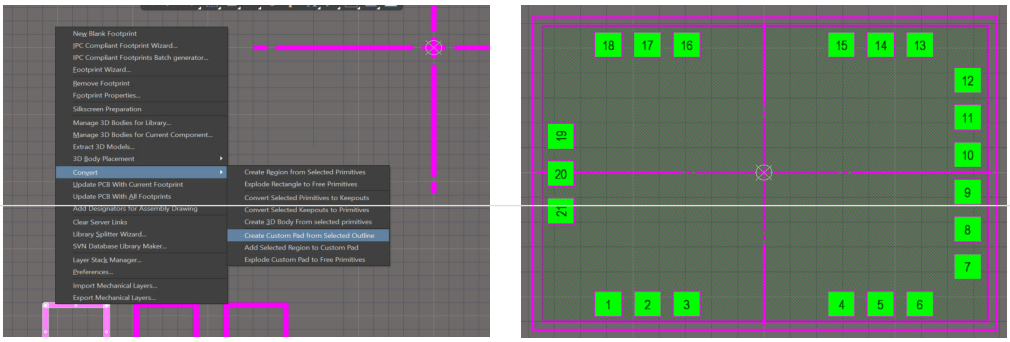


Figure 19. Die pad creation

STEP 3: Adding wire bonding "landing/finger pads"

Next step is to add the wire bonding landing (aka finger) pads, i.e. the pads where the bond wire from the die pads will connect to. These pads are also referred to as "finger" pads. The pads will have to be located on the copper layers (top or bottom) which then can be routed to the rest of the design.

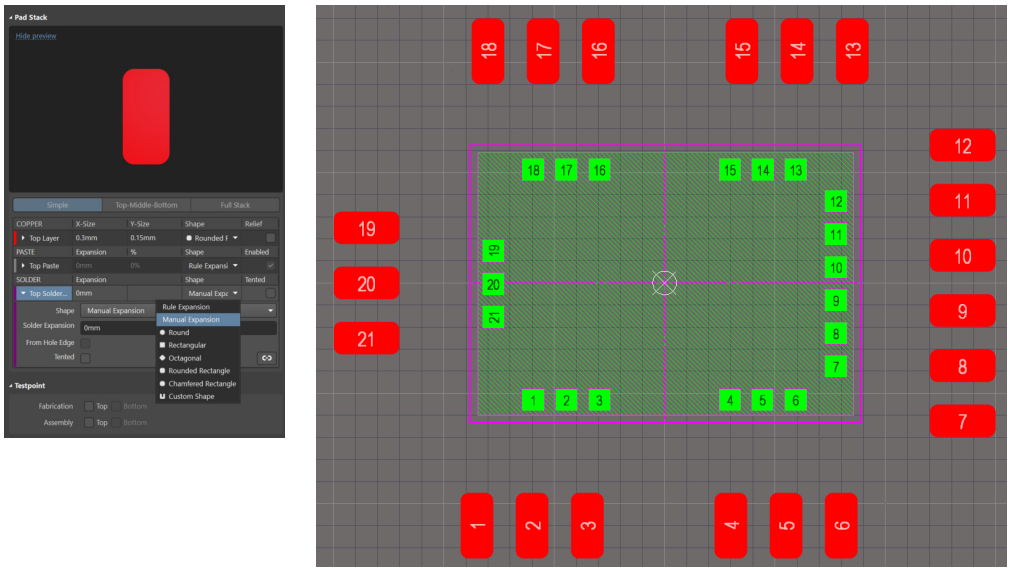


Figure 20. Finger pad creation

The dimensions of the pads and their pitch depends on whether “wedge” or “ball” bonding is used. In wedge bonding the pads’ width can be narrow, approximately two times the diameter of the wire, whereas the pads length needs to be approximately four times the diameter of the wire to accommodate the wedge bond. The distance of the pads from the die depends on the die thickness and dimensions, additionally the pads might have to be staggered especially for designs with a high number of bond wires.

Additionally, as a general requirement for the wire bonding is that the pads should have no solder mask around them and in between them. We will define the solder mask expansion around all the pads with a fill zone, and so for now for each pad we need to set its solder mask expansion rule to “Manual Expansion” with a value of 0mm.

STEP 4: Drawing the bond wires

We can now begin to ‘draw’ the bond wires from chip’s pads to the landing pads. This can be done manually by drawing lines (Place → Bond Wire) on the dedicated “Wire Bonding” layer.

The geometrical properties of the bond wire, such as diameter, loop height and bond type can be controlled in the properties panel. Make sure to view the bond wire in 3D view to make sure they are set correctly.

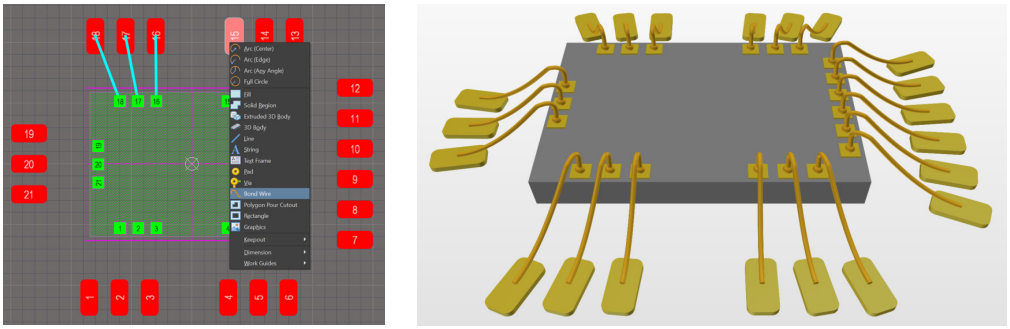


Figure 21. Wire bond placement

STEP 5: Pad alignment and orientation

Depending on the wire bonding technology used and the material of wire, for example gold wire bonding, it may be required to adjust the orientation of the pad with respect to the die so that the pad aligns with the direction of the bond wire. Altium Designer is able to automatically align the pads with the direction of the bond wire.

To use this feature, first select all the bond pads and the wire bonds. Then position your mouse cursor above any pad and right click to access the Pad Actions menu and select Align Bond Finger with Bond Wire under the Pad Actions menu.

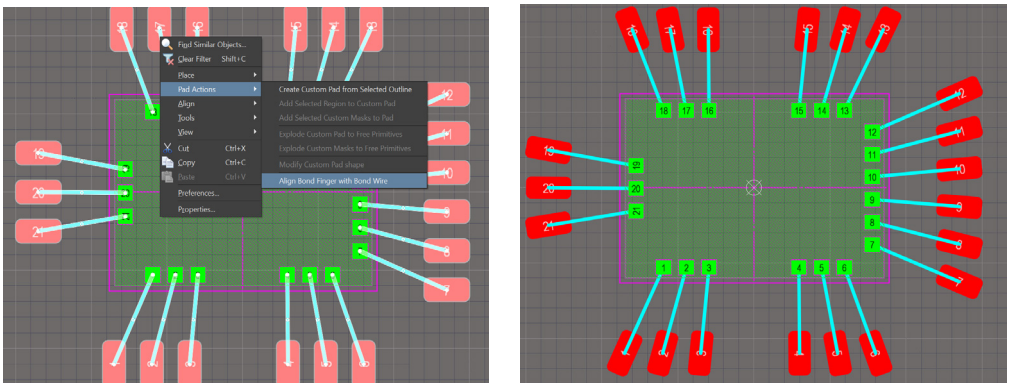


Figure 22. Pad alignment

STEP 6: Removing solder mask along the pads

Solder mask around and in between the pads and in between must be removed. This can be done by switching to the solder mask layer associated with the pads and placing a fill around the pads.

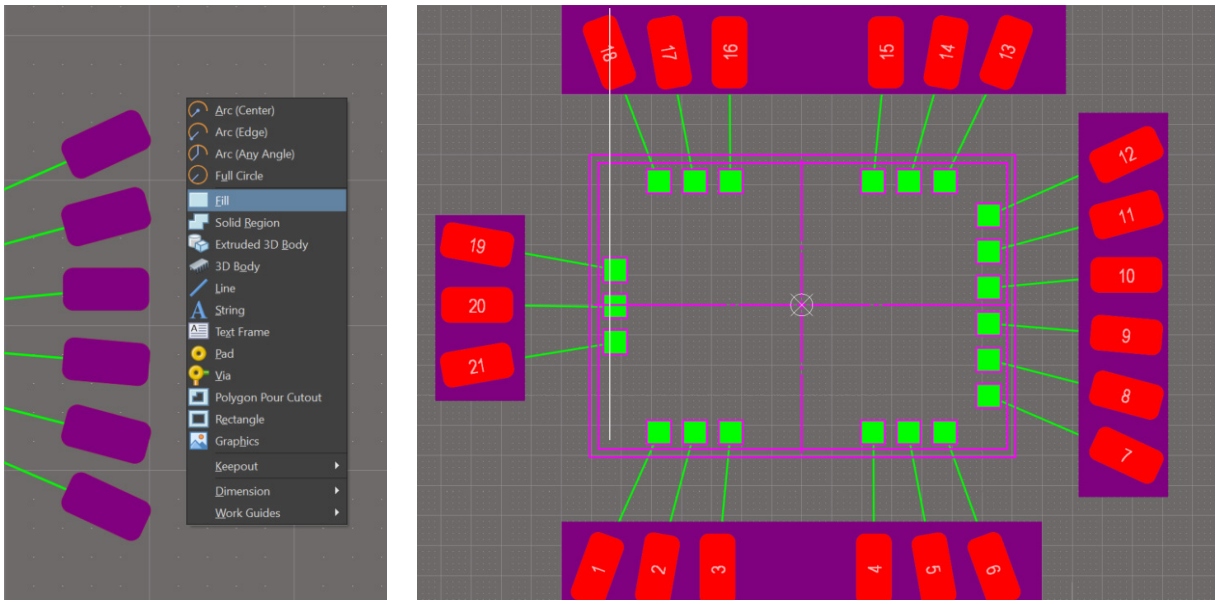


Figure 23. Soldermask removal

STEP 7: Keep-outs and courtyards

Placement of components on the other side of the board directly behind the die position may not be allowed by the manufacturer. This is because a bond tool fixture is attached underneath the die position to hold the board in place while the die is positioned, and the wire bonding is in process. In Altium Designer a “Keepout zone” can be placed on the opposite side of the board to prevent any components from being placed during the layout and routing of the board.

Glob top encapsulation and coatings are used to protect the die and bond wires. A courtyard can also be placed around the die and pads to account for glob top.

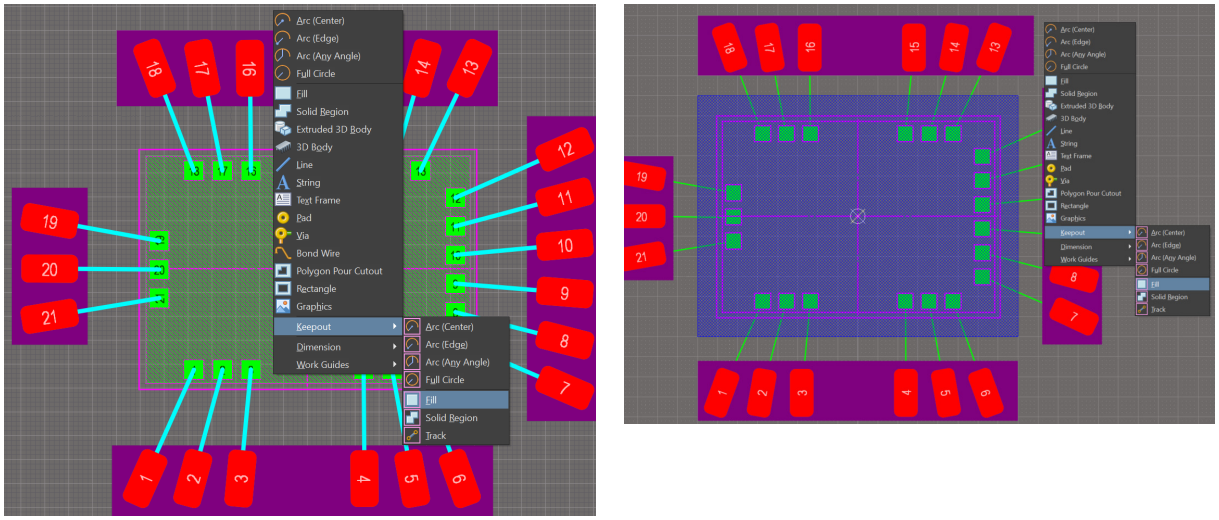


Figure 24. Placing keepouts and courtyards

STEP 8: Generating Output Report and Draftsman Drawings

After completing the routing of your design, assembly and fabrication drawings showing the COB and its wire bonds can be done in Draftsman. Ensure that “Die” and “Wire Bond” components pair layers that were created in STEP2 are enabled in the properties panel of each view.

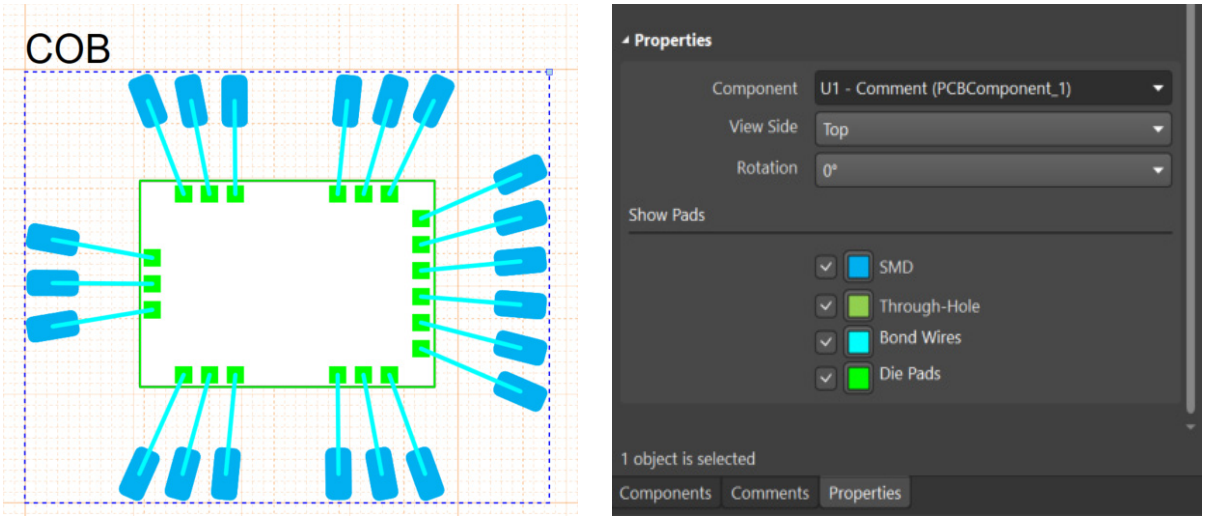


Figure 25. Draftsman component view and properties settings of the COB and its wire bonds

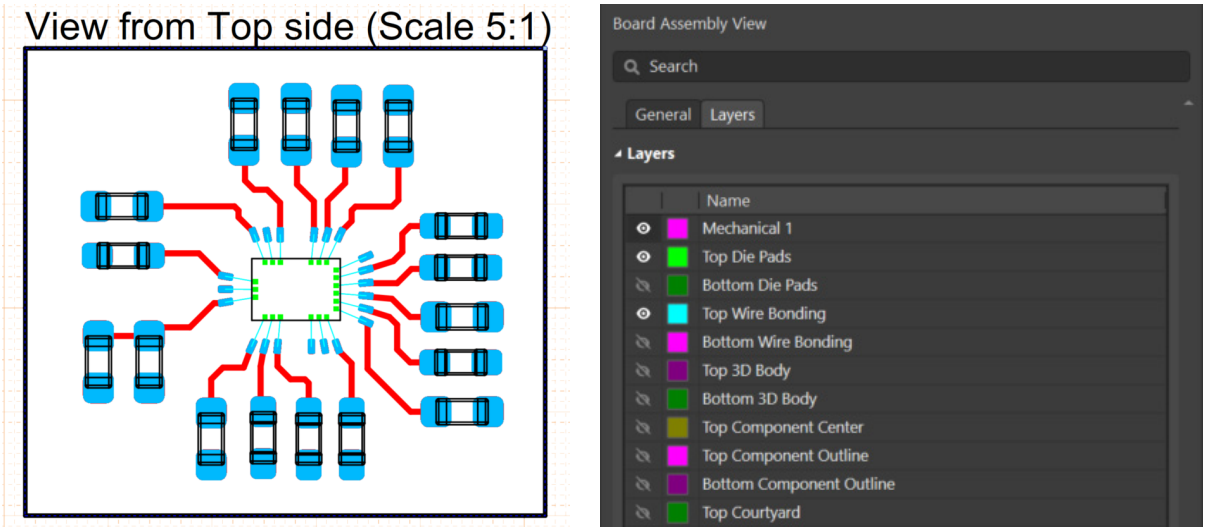
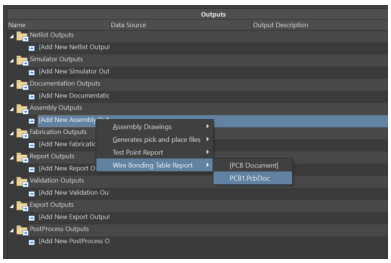


Figure 26. Draftsman assembly view and properties setting showing all components and the COB

Additionally Altium Designer can generate a table report (in CSV format) describing all the wire bond connections including die pads names and designators, along with dimensions. This data can be required by wire bonding service providers and manufacturers. This report can be set up in the Outjob file as shown below.



	A	B	C	D	E	F	G	H	I	J	K	L	M
1	Wire Start	X [mm]	Y [mm]	Net	Die Pad Size X [	Die Pad Size Y [mm]	Wire End	X [mm]	Y [mm]	Wire Diam	Wire Length [mm]	Loop Height [mm]	Type
2	Pad U1-1	99.609	85.83	U1-1	0.1	0.1	Pad U1-1	99.353	85.26	0.025	0.878	0.15	Ball
3	Pad U1-2	99.759	85.83	U1-2	0.1	0.1	Pad U1-2	99.603	85.26	0.025	0.849	0.15	Ball
4	Pad U1-3	99.908	85.83	U1-3	0.1	0.1	Pad U1-3	99.853	85.26	0.025	0.833	0.15	Ball
5	Pad U1-4	100.498	85.83	U1-4	0.1	0.1	Pad U1-4	100.503	85.26	0.025	0.831	0.15	Ball
6	Pad U1-5	100.647	85.83	U1-5	0.1	0.1	Pad U1-5	100.753	85.26	0.025	0.839	0.15	Ball
7	Pad U1-6	100.797	85.83	U1-6	0.1	0.1	Pad U1-6	101.003	85.26	0.025	0.861	0.15	Ball
8	Pad U1-7	100.98	85.982	U1-7	0.1	0.1	Track	101.553	85.735	0.025	0.877	0.15	Ball
9	Pad U1-8	100.98	86.132	U1-8	0.1	0.1	Track	101.553	85.985	0.025	0.849	0.15	Ball
10	Pad U1-9	100.98	86.282	U1-9	0.1	0.1	Pad U1-9	101.553	86.235	0.025	0.835	0.15	Ball
11	Pad U1-10	100.98	86.432	U1-10	0.1	0.1	Pad U1-10	101.553	86.485	0.025	0.835	0.15	Ball
12	Pad U1-11	100.98	86.582	U1-11	0.1	0.1	Pad U1-11	101.553	86.735	0.025	0.85	0.15	Ball
13	Pad U1-12	100.98	86.732	U1-12	0.1	0.1	Pad U1-12	101.553	86.985	0.025	0.879	0.15	Ball
14	Pad U1-13	100.797	86.874	U1-13	0.1	0.1	Pad U1-13	101.053	87.41	0.025	0.851	0.15	Ball
15	Pad U1-14	100.648	86.874	U1-14	0.1	0.1	Track	100.803	87.41	0.025	0.821	0.15	Ball
16	Pad U1-15	100.498	86.874	U1-15	0.1	0.1	Pad U1-15	100.553	87.41	0.025	0.805	0.15	Ball
17	Pad U1-16	99.908	86.874	U1-16	0.1	0.1	Track	99.903	87.41	0.025	0.802	0.15	Ball
18	Pad U1-17	99.758	86.874	U1-17	0.1	0.1	Pad U1-17	99.653	87.41	0.025	0.811	0.15	Ball

Figure 27. Table report generation

7.2. Further examples and use cases

The previous design example showed the basic functionality of Altium Designer's integrated Wire Bonding tool. The tool is capable of much more, below are some examples and use cases. Note that we will be using the Wire Bonding tool directly within the PCB document file.

- **Wire bonding to a copper pour**

Some components such as chip capacitors and power semiconductors require wire bonds from the die pads to a copper pour on the PCB. Altium Designer Wire Bonding tool now allows to place wire bonds straightforwardly on copper pours during the PCB design process.

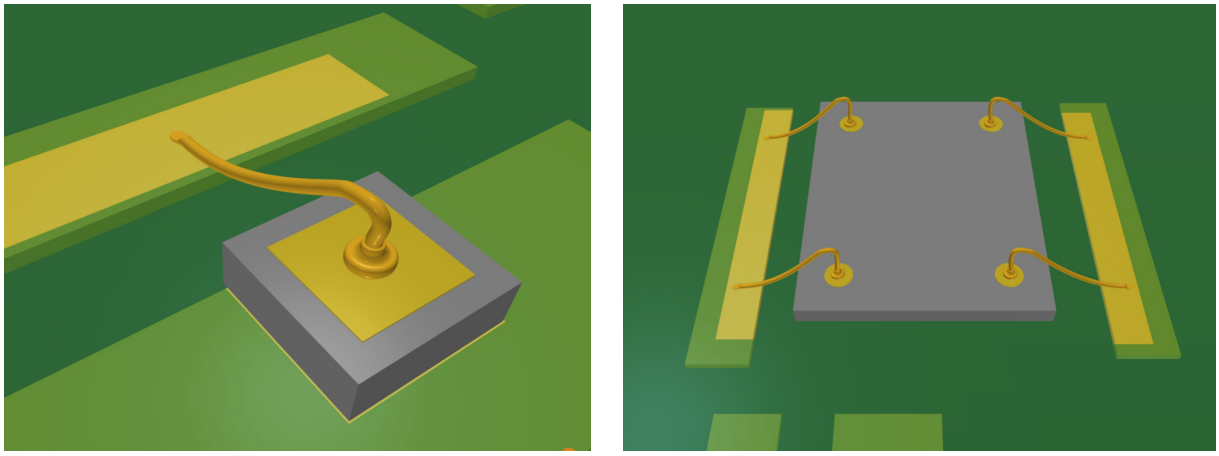


Figure 28. Wire bonding on copper pours for silicon chip capacitors

- **Die-to-die wire bonding**

In high density and layout-sensitive designs, such as high frequency RF and power electronics, minimizing the connection loops and area is key to reduce the effect of parasitic inductances and capacitances on performance. Altium Designer's Wire Bonding tool allows for directly placing wire bonds between dies pads on different dies, without the need for an intermediate finger pads.

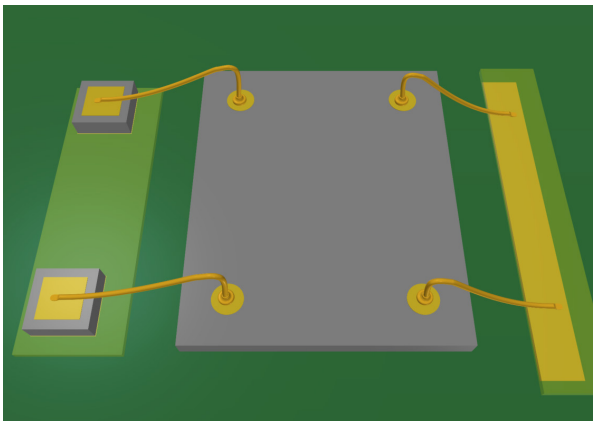


Figure 29. Die-to-die wire bonding for RF silicon capacitors

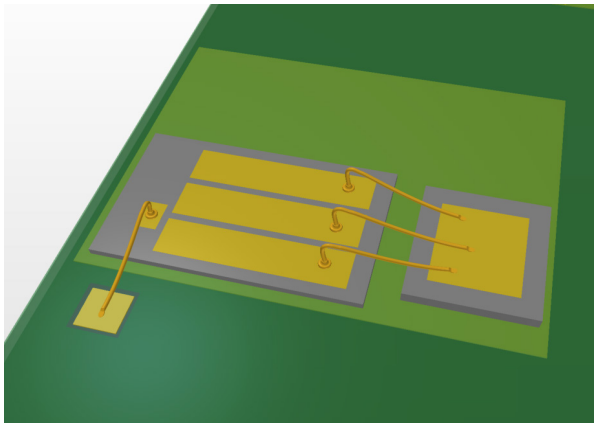


Figure 30. Die-to-die wire bonding for power semiconductors

- **Multiple wire bonds for the same die pad**

Having multiple wire bonds connected to the same die may be necessary in some applications to increase the carrying capacity and to reduce the total impedance (resistance and inductance) from the die pad to the PCB. Altium Designer's Wire Bonding tool allows for placing multiple wire bonds on the same die pad when either creating a library component or during PCB editing.

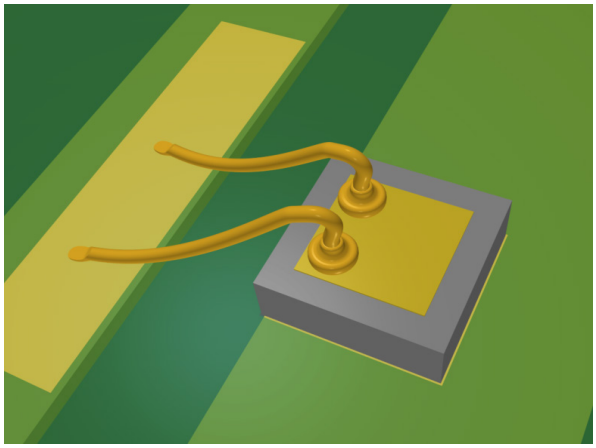


Figure 31. Multiple wire bonds for an RF silicon capacitor to lower impedance

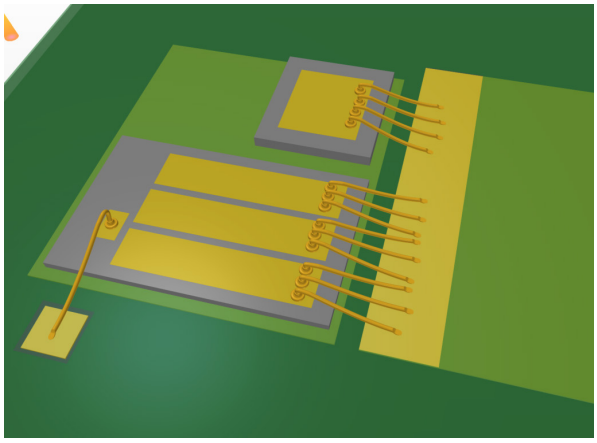


Figure 32. Multiple wire bonds in power semiconductors to increase the current carrying capacity

- **Wire bonding control in 3D view**

With Altium Designer's advanced 3D viewing and modeling capabilities, wire bonds can also be adjusted and controlled in 3D view without having to switch back and forth between 2D and 3D layout views. You can control and visualize the changes in the wire bond's properties - location and length, and its profile such as loop height, diameter and bond type.

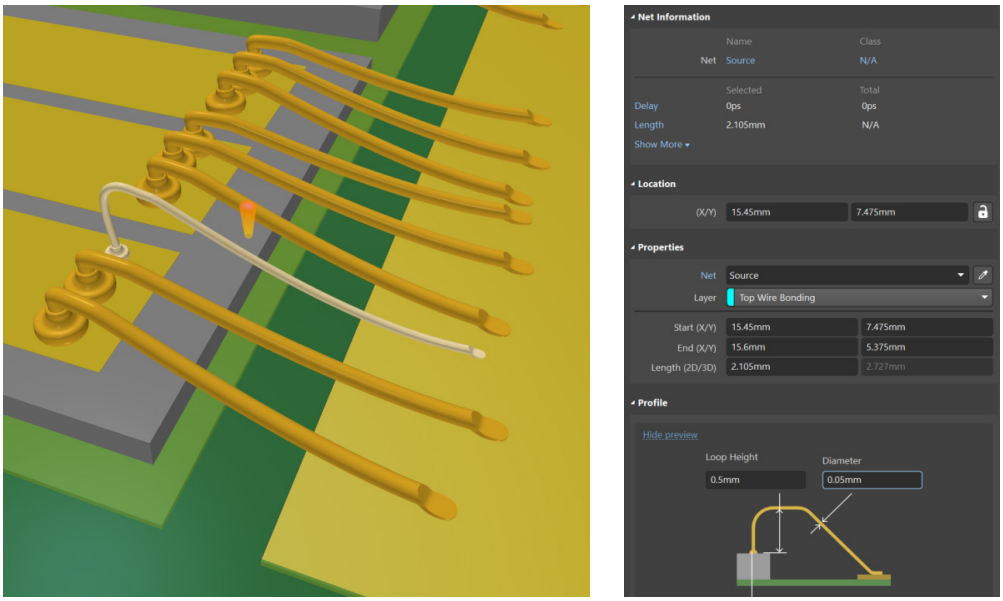


Figure 33. Wire bonds can be selected and configured in 3D layout view

- **Wire bond length measurement**

When placing wire bonds, Altium Designer will automatically calculate the wire bond length in 2D and 3D. 2D length is the wire bond's distance from its first connection to the die pad to its second connection to the finger pad or PCB copper. 3D length is the actual wire bond length, i.e. the distance along the wire bond, taking into account the loop height. These measurements can be useful to determine if the wire bond's lengths are within the limits of the chosen wire bonding technology and the capabilities of the manufacturer, especially in designs that have multiple wire bond rows.

The 2D and 3D length measurements can be read in the Properties panel of the selected wire bond.

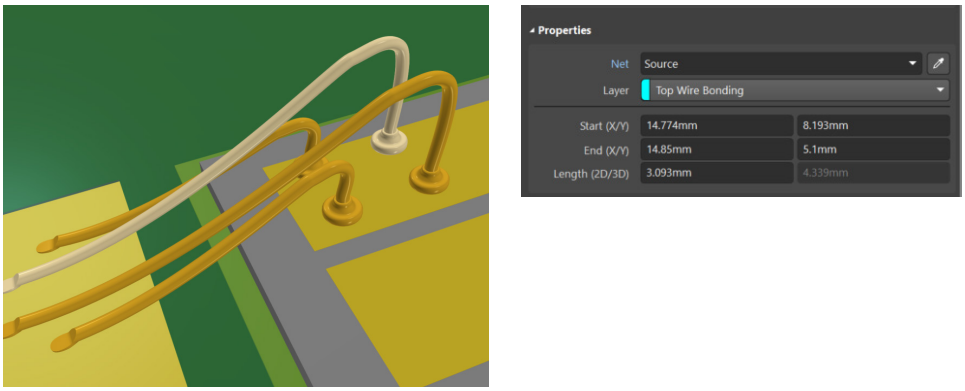


Figure 34. Wire bond length measurements can be accessed in the properties panel

- **Wire Bonding Stacked Die and Die in Cavity - “3D Integrated Circuits”**

The Wire Bonding tool in Altium Designer is capable of handling advanced and complex designs such as stacked die and die in cavity. These new designs, sometimes referred to as 3D Integrated Circuits, allow for achieving compactness and high compute power density.

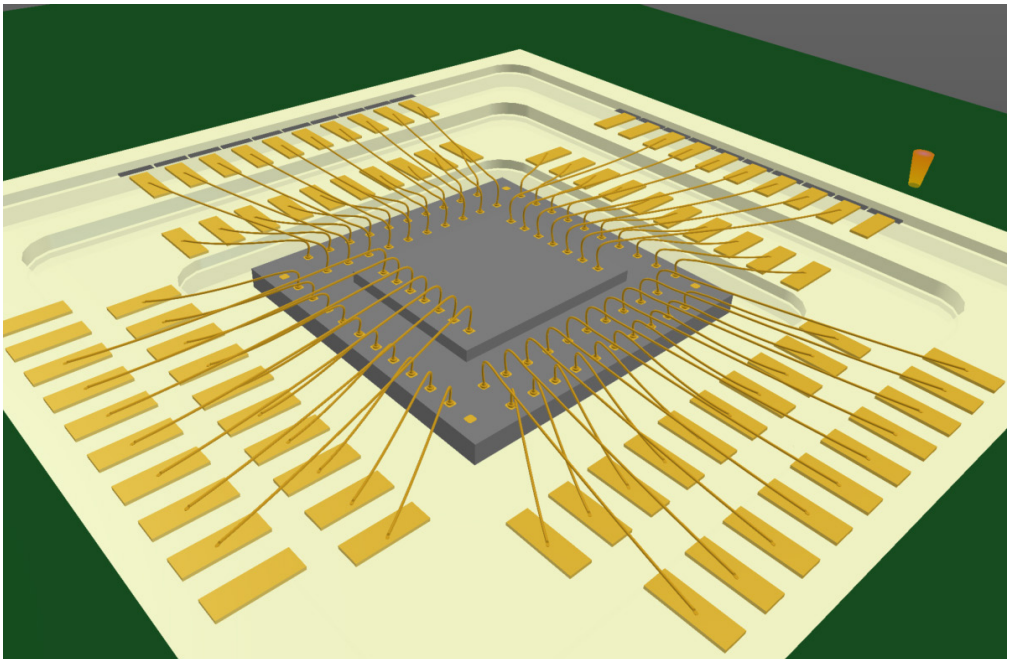


Figure 35. Wire bonding stacked die in the cavity (3D Integrated Circuit) design in Altium Designer

Altium Designer has the capability to model PCB cavities and embedded components, this can be first done via using the Rigid & Flex Advanced Mode in the Layer Stack Manager. Multiple board stacks can be defined to represent the individual stacks that the bare die and fingers pads will be on. The stacks can then be drawn in the Board Planning Mode and their order priorities can be set. The following shows the individual steps to create a two vertically stacked die in a cavity with finger pads distributed on two internal layers.

First enter the Layer Stack Manager and select the Rigid & Flex Advanced Mode, and create three additional stacks as shown below. The “Main” stack of the PCB contains 6 copper layers. The “Finger Pads 1” stack begins with internal layer Mid 2 and will contain the first layer of the finger pads. The “Finger Pads 2” stack begins with internal layer Mid 3 and will contain the next layer of finger pads. The “Die” stacks begin with internal layer Mid 4 and will contain the stacked die.

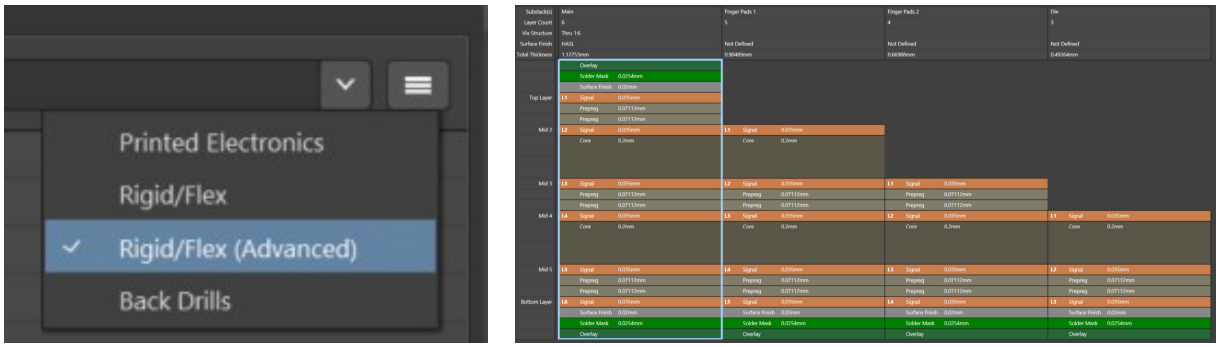


Figure 36. Using the Rigid & Flex Advanced Mode in the Layer Stack Manager to create three additional stacks.

Next, in the board planning mode we can now draw the individual stacks and set their priorities as shown below

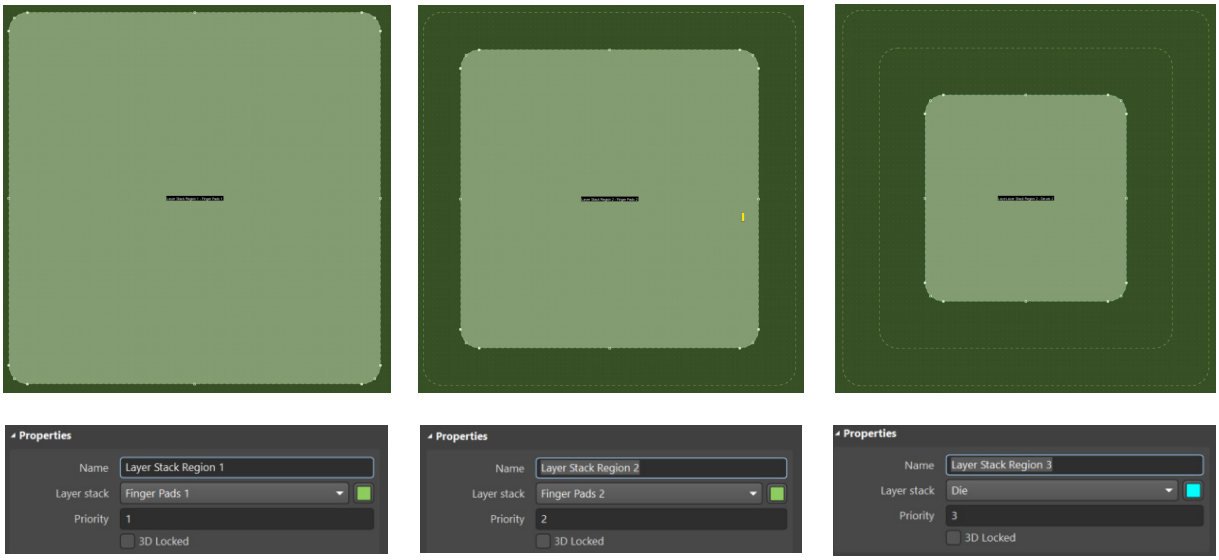


Figure 37. Drawing the “Finger Pads 1” stack and assigning a Priority of 1

Figure 38. Drawing the “Finger Pads 2” stack and assigning a Priority of 2

Figure 39. Drawing the “Die” stack and assigning a Priority of 3

Next, we can now place the finger pads and the die. These can be defined as library components or drawn directly in PCB mode, and subsequently the wire bonds can then be drawn as shown below

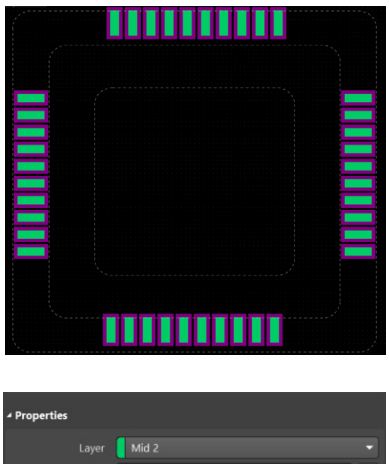


Figure 40. Placing the first layer of finger pads on Layer Mid 2.

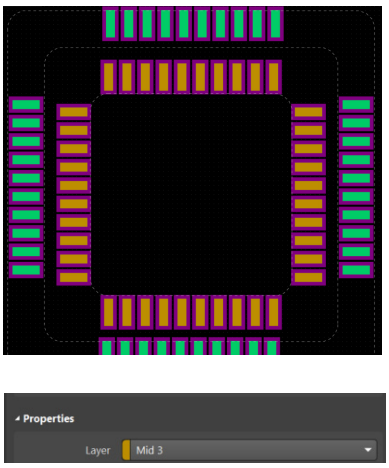


Figure 41. Placing the next layer of finger pads on Layer Mid 3

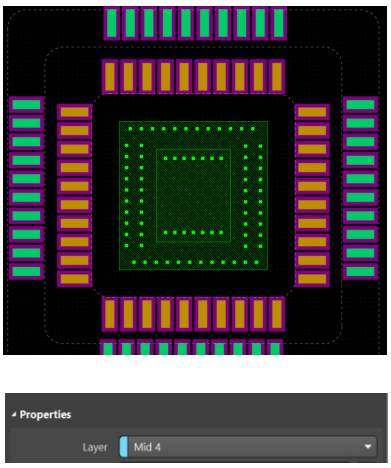


Figure 42. Placing the die body on Layer Mid 4.

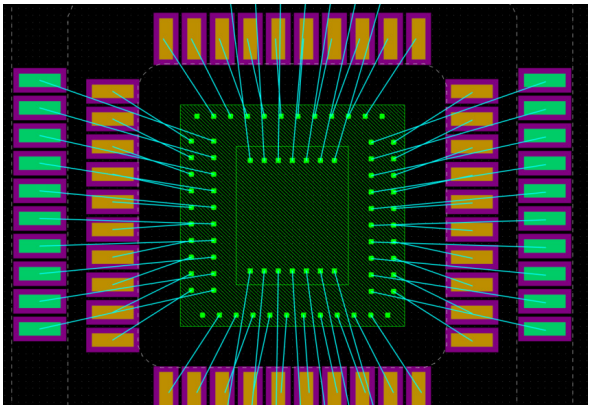


Figure 43. Place wire bonds wire, adjust wire bond loop height settings accordingly

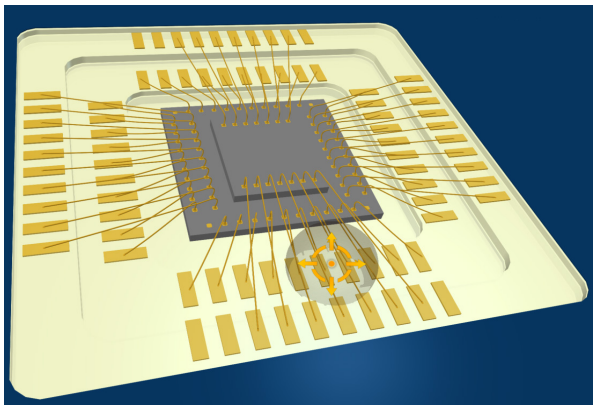


Figure 44. View your design in 3D mode. In some cases the transparency of the solder mask layer should be set to max

- **Design Rules Checks for Wire Bonding**

Altium Designer's now allows you to set design rule checks (DRC) and constraints specifically for Wire Bonding. The new Wire Bonding rule can be found under the Routing category and can be programmed to check for 'wire to wire' clearance, bond finger margin, and minimum and maximum bond wire lengths.

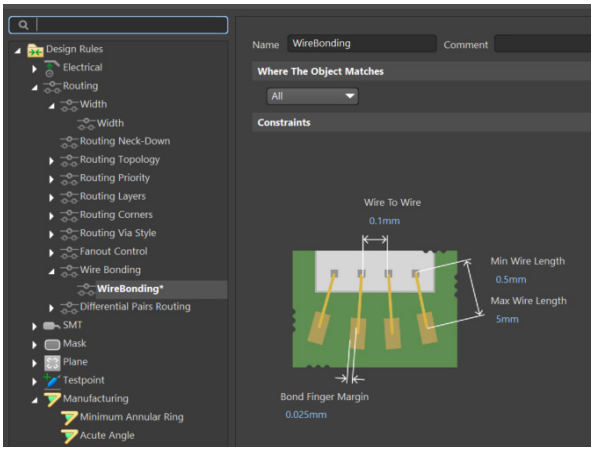


Figure 45. The new Wire Bonding design rules in Altium Designer

When running the Wire Bonding DRC, Altium Designer will flag and highlight any violations that it finds in 2D and 3D. To run the Wire Bonding DRC, access the PCB Rules and Violations Panel and select Wire Bonding, then right-click and select 'Run DRC Rule Class' (Wire Bonding). Any violations found will be listed in the text box below along with the exact details of the violation. Wire bond violations can also be seen in 3D view and will be highlighted in green.

In the example below, Altium Designers has found a "wire to wire" violation indicating that the distance between the two wire bonds on the same pad is less than the minimum required distance set in the Wire Bonding design rule.

Note that Electrical rule checks (Un-Routed Net and Short Circuit) also apply to Wire Bonding.

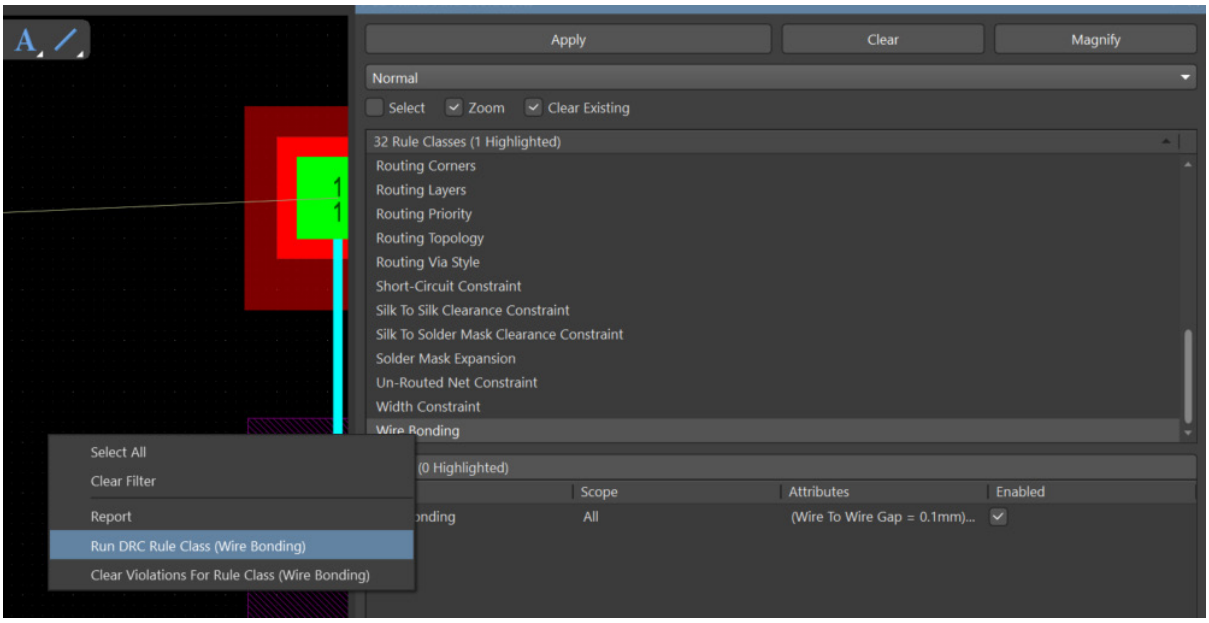


Figure 46. Running the Wire Bonding design rule

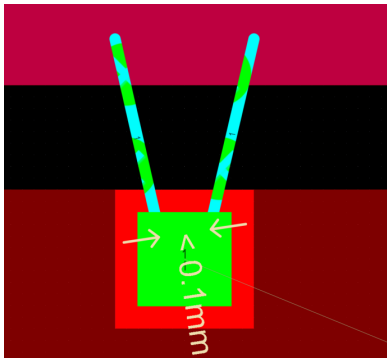


Figure 47. Flagged 'wire to wire' violation in 2D view

Figure 48. Violation details are listed in the text box

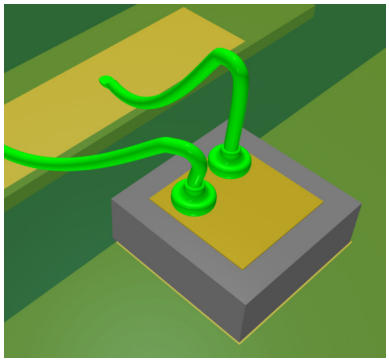


Figure 49. Flagged violation in 3D view

- **Query Language and DRC**

Altium Designer now has two new query language keywords that can be used in logical query expressions when creating design rule scopes, in both the Constraint Manager and the PCB Rules and Constraints Editor.

IsBondFinger – returns an SMD pad primitive that has a bond wire connected to it.

IsBondWireConnected – returns any primitive that has a bond wire connected to it.

Both of these keywords can be used in the Constraint Manager and the PCB Rules and Constraints Editor.

For example, we can create a clearance DRC that would only apply to the finger pads used for wire bonding as shown below. Due to the rotation of the pads to be aligned with the wire bonds, this may cause some pads to become closer to each other.

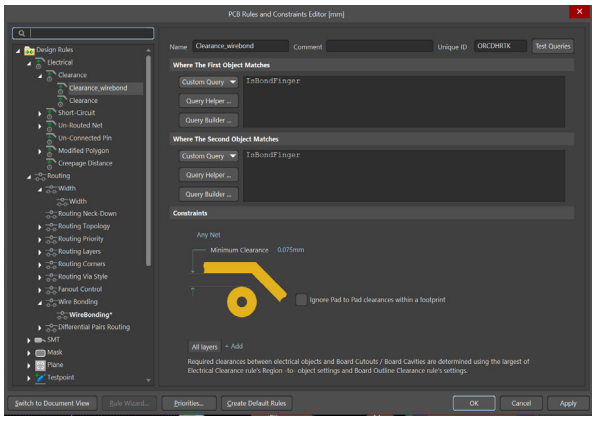


Figure 50. Defining a 75 um clearance DRC only for the finger pads using the IsBondFinger keyword

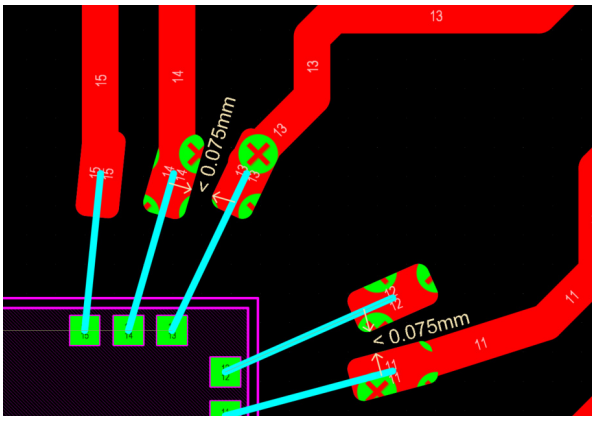


Figure 51. Flagged finger pad clearance violation

We can also create another clearance DRC for primitives other than finger pads that have wire bond connections. For instance we would like to specify a clearance DRC on copper pours that have a wire bond connection to other primitives. The extra clearance might be needed as those copper pours will be exposed (i.e. without solder mask). This can be done as shown below

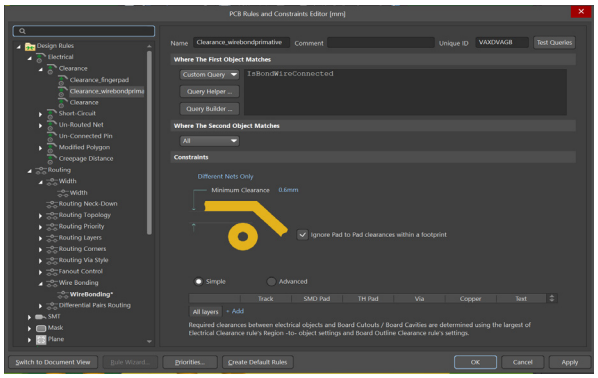


Figure 52. Defining a 0.6 mm clearance DRC only for primitives using the IsBondWireConnected keyword

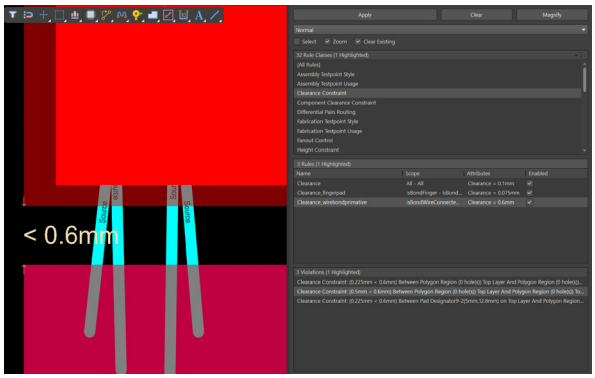


Figure 53. Flagged finger pad clearance violation. The PCB Rules and Violations panel list the details of the violation

7.3. Wire bonding for Altium Designer (pre AD2X)

> NOTE:
> that Altium Designer 20 and above with a Standard subscription level are required.

This section describes how to set up wire bonding in Altium Designer (pre AD2X). The image below shows the COB design that we will aim to create

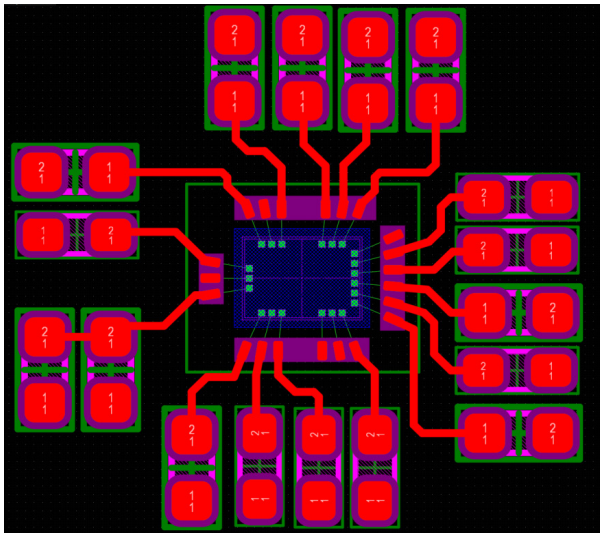


Figure 54. The COB with wire bonding design example in Altium Designer (Pre-AD2X)

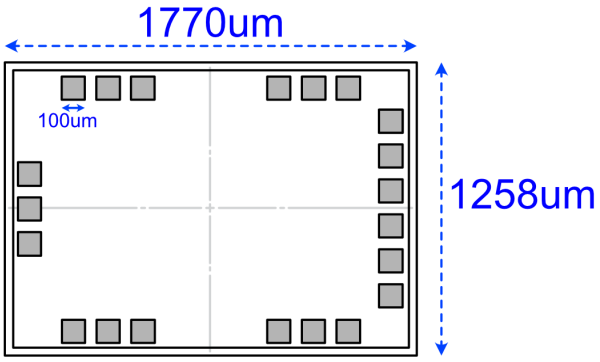


Figure 55. Bare Die drawing

STEP 1: Footprint creation & Importing die graphics

First step is to create a die footprint which can then be used to create track connections to the rest of the circuitry. Similar to any other component, the footprint for the die can be added to an existing library that is either an integrated library or a project library. Alternatively a new library file can be created specifically for chip-on-board dies.

The footprint creation process begins first with the assumption that you have a CAD file for the die that includes the outline of the die body, its pads, and their locations. The die in the image below will be used for this guide, its dimensions are 1770um x 1258um and has twenty one pads each with a dimension of 100um x 100um.

Altium Designer can import CAD data which contains outlines of the die and its pads in the form of a DXF file. The DXF import settings allow you to choose the correct units, and on which layer to place the imported data. Once the import process is complete, it is recommended that the measuring tool is used to verify that the imported CAD data has the correct dimensions. The imported CAD data might need to be repositioned to be at the origin, and finally the imported data can be locked to prevent them from being modified or moved.

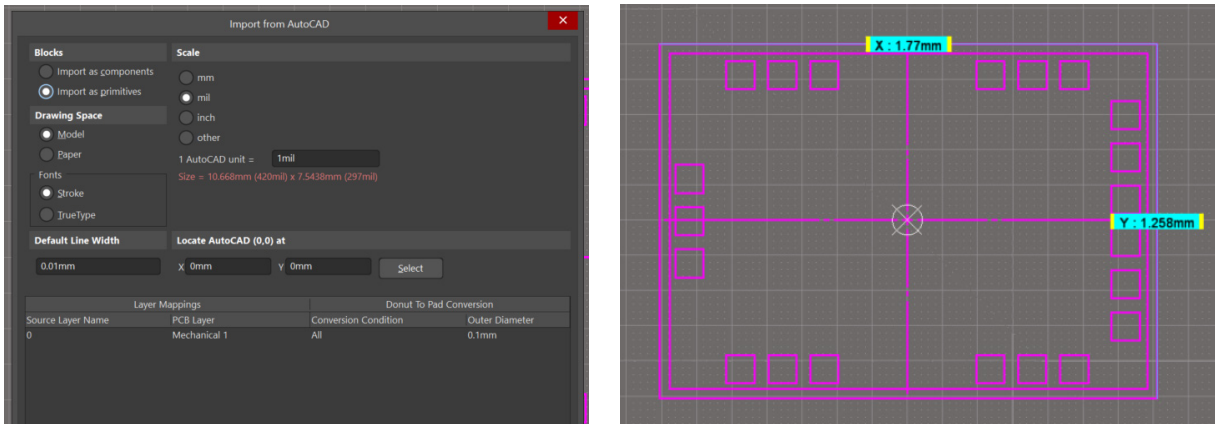


Figure 56. CAD data import

STEP 2: Wire bonding “Data Layer”

The data associated with wire bonding may need to be included in the output and fabrication for the manufacturer to process. Altium Designer does not have a dedicated layer for the primitives associated with wire bonding such as the bond wires, the pads on the die and bond wire landing pads however it is possible define these primitives in a mechanical layer which then can be included in the fabrication output data.

In the footprint editor, a new mechanical layer can be added as the wire bonding data layer. This layer can be used to place all the primitives related to wire bonding.

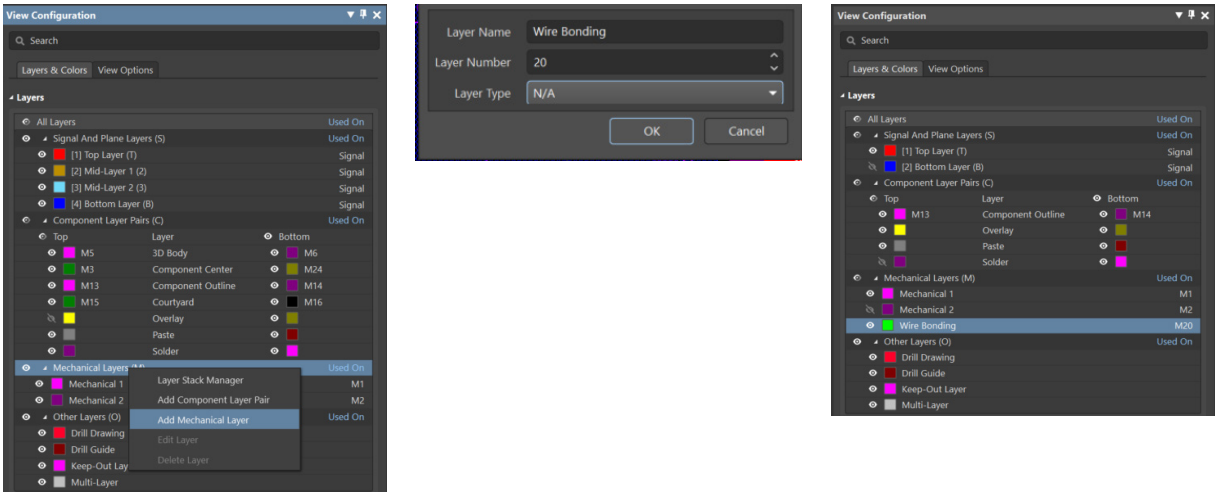


Figure 57. Die and wire bonding layers

Starting with pads on the chip, we can now move those to our “Wire Bonding” mechanical layer. If the pads have been as outlines, then these can be converted to “regions” and then moved to the “Wire Bonding” mechanical layer.

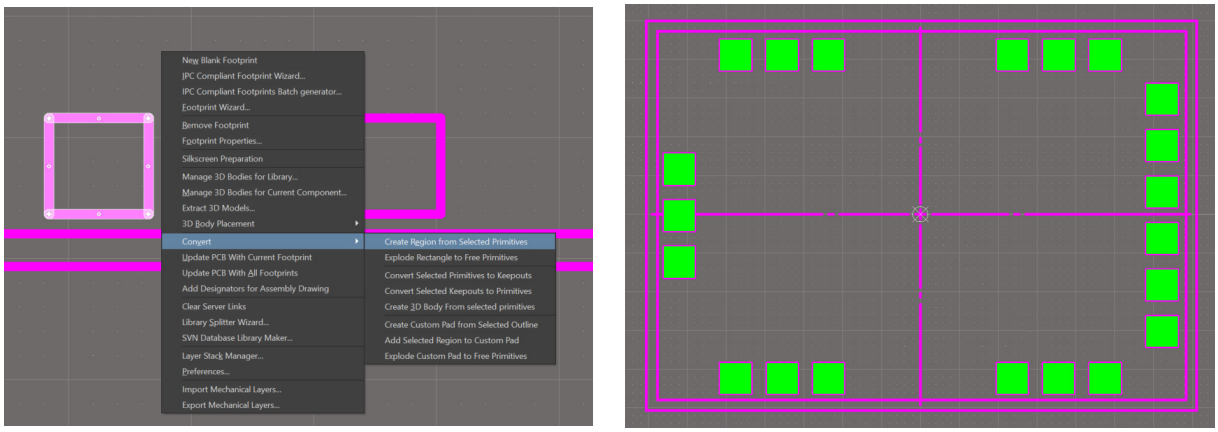


Figure 58. Die pad creation

Other primitives such as the die outline, center positions can also be included in the Wire Bonding layer (or other layers), check with your wire bonding manufacturer for what data is required.

STEP 3: Adding wire bonding landing (finger) pads

Next step is to add the wire bonding finger pads, i.e. the pads where the bond wire from the die pads will connect to. These pads are also referred to as “finger” pads. The pads will have to be located on the copper layers (top or bottom) which then can be routed to the rest of the design. The pads will also have to be duplicated and located on the “Wire Bonding” mechanical layer so that the bond wire can be then ‘drawn’ to the pads on the die.

The dimensions of the pads and their pitch depends on whether “wedge” or “ball” bonding is used. In wedge bonding the pads’ width can be narrow, approximately two times the diameter of the wire, whereas the pads length needs to be approximately four times the diameter of the wire to accommodate the wedge bond.

Additionally, as a general requirement for the wire bonding is that the pads should have no solder mask around them and in between them. We will define the solder mask expansion around all the pads with a fill zone, and so for now for each pad we need to set its solder mask expansion rule to “Manual Expansion” with a value of 0mm.

The pads’ positions with respect to the die itself depends on the specifics of the wire bonding capabilities of the PCB manufacturer, however in general the location of the pads with respect to the die depends on the die’s thickness, it is generally 1.3 to 1.5 times the die’s thickness. It can be useful to draw lines on a mechanical layer to function as guides for placing the pads.

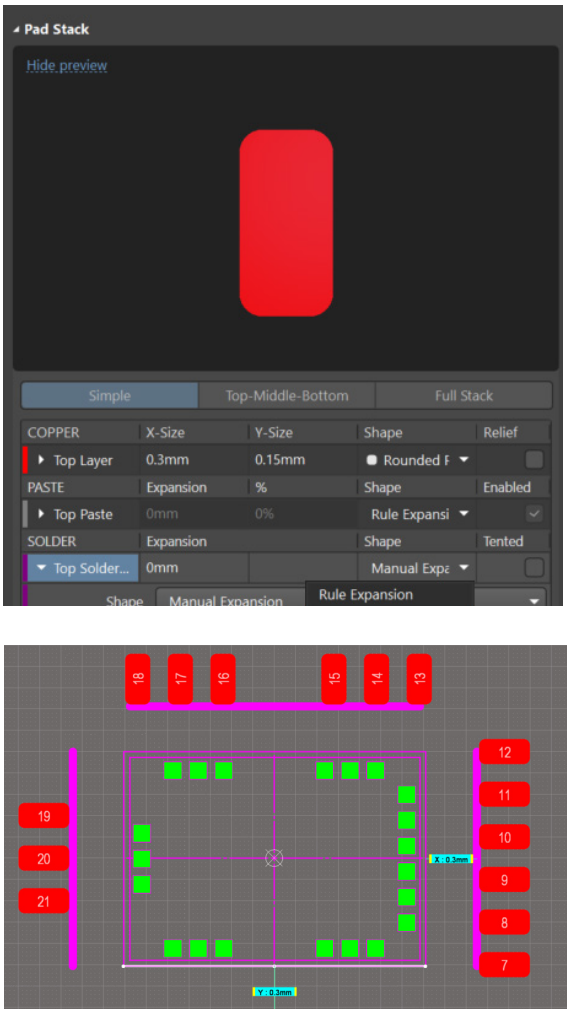


Figure 59. Finger pads creation

Once the finger pads have all been placed, they now need to be duplicated and moved to the “Wire Bonding” mechanical layer.

TIP: to duplicate the pads, select all of them first, and then copy (CTRL+C) them and pick a reference point (such as the origin). Do not clear the selected pads yet. Then paste the pads (CTRL+V) at the same reference point that was initially used. You now have duplicated pads that are on top of each other and on the same layer whilst the original pads are still selected. Since the original pads are still selected, you can now set those to be on the “Wire Bonding” mechanical layer.

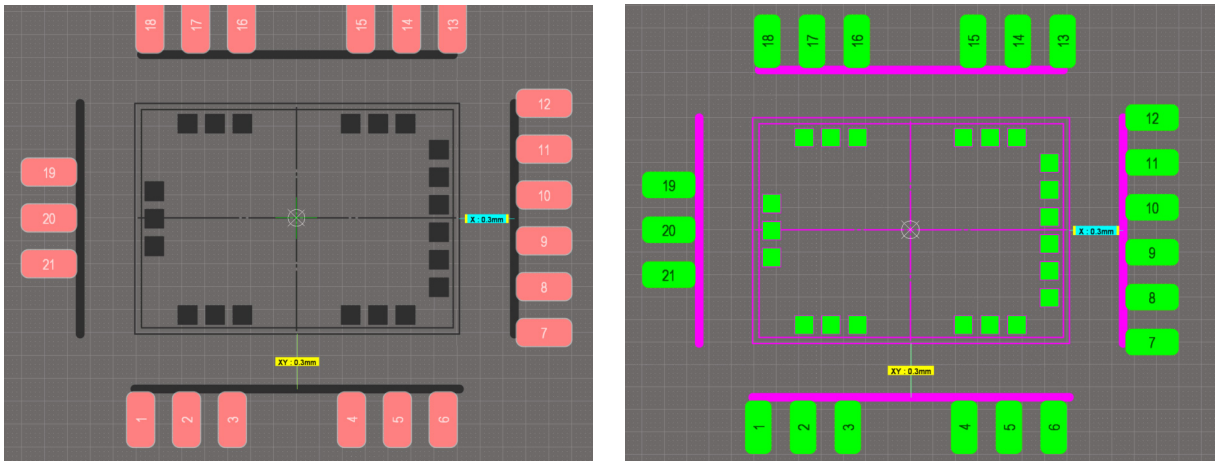


Figure 60. Moving finger pads to the wire bonding mechanical layer

STEP 4: Drawing the bond wires

We can now begin to ‘draw’ the bond wires from chip’s pads to the landing pads. This can be done manually by drawing lines (Place → Line). Press SHIFT+SPACE to use ‘AnyAngleMode’ to draw the lines and enable snapping to ensure the lines snap to the landing pads. The line width can be set to the bond wire diameter.

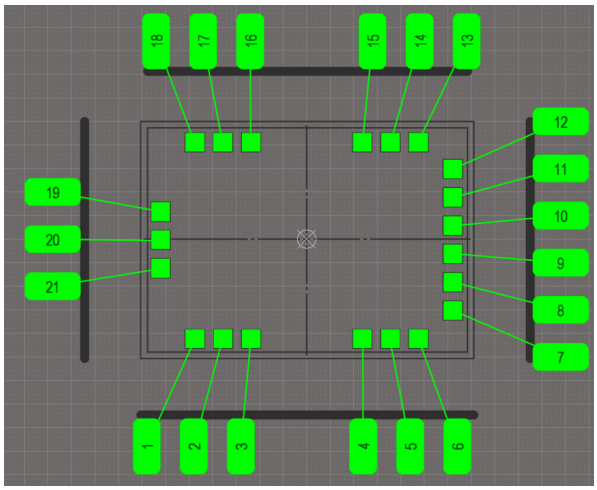


Figure 61. Drawing the bond wires

STEP 5: Pad alignment and orientation

Depending on the wire bonding technology used and the material of wire, for example gold wire bonding, it may be required to adjust the orientation of the pad with respect to the die so that the pad aligns with the direction of the bond wire. The rotation in each pad can be set manually in the pad's property panel.

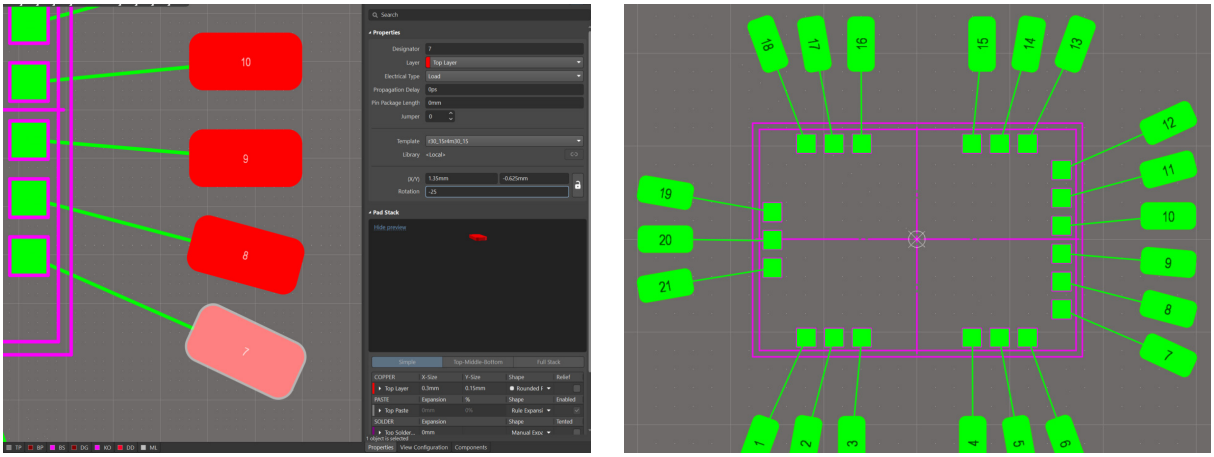


Figure 62. Pad alignment and rotation

STEP 6: Removing solder mask along the pads

Solder mask around and in between the pads and in between must be removed. This can be done by switching to the solder mask layer associated with the pads and placing a fill around the pads.

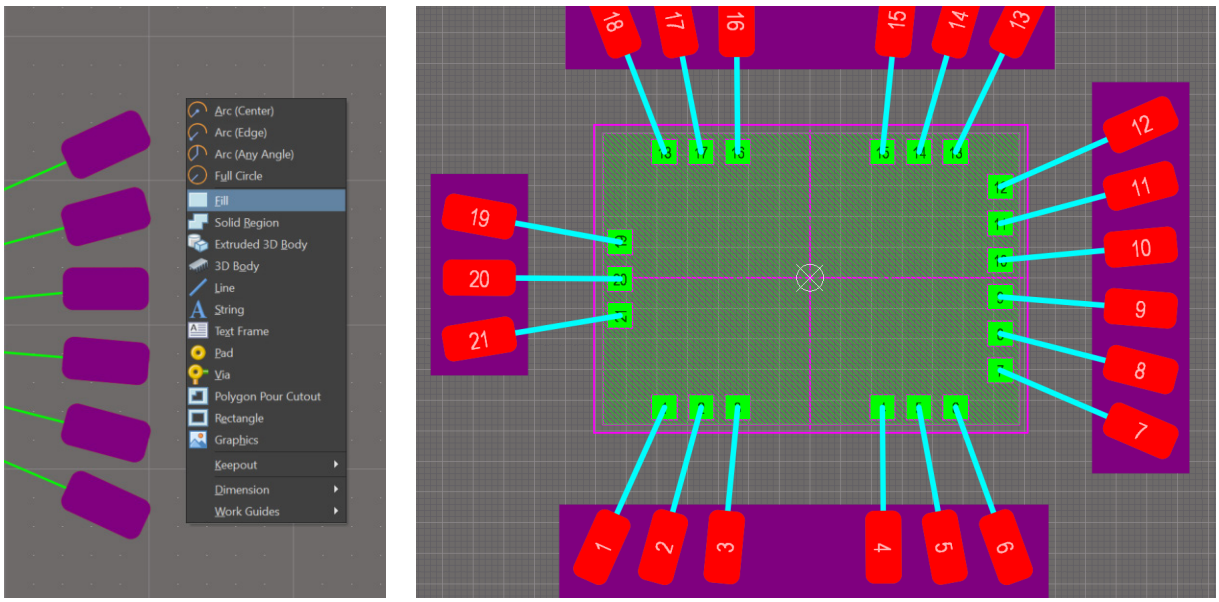


Figure 63. Soldermask removal

STEP 7: Keep-outs and courtyards

Placement of components on the other side of the board directly behind the die position may not be allowed by the manufacturer. This is because a bond tool fixture is attached underneath the die position to hold the board in place while the die is positioned, and the wire bonding is in process. In Altium Designer a “Keepout zone” can be placed on the opposite side of the board to prevent any components from being placed during the layout and routing of the board.

Glob top encapsulation and coatings are used to protect the die and bond wires. A courtyard can also be placed around the die and pads to account for glob top.

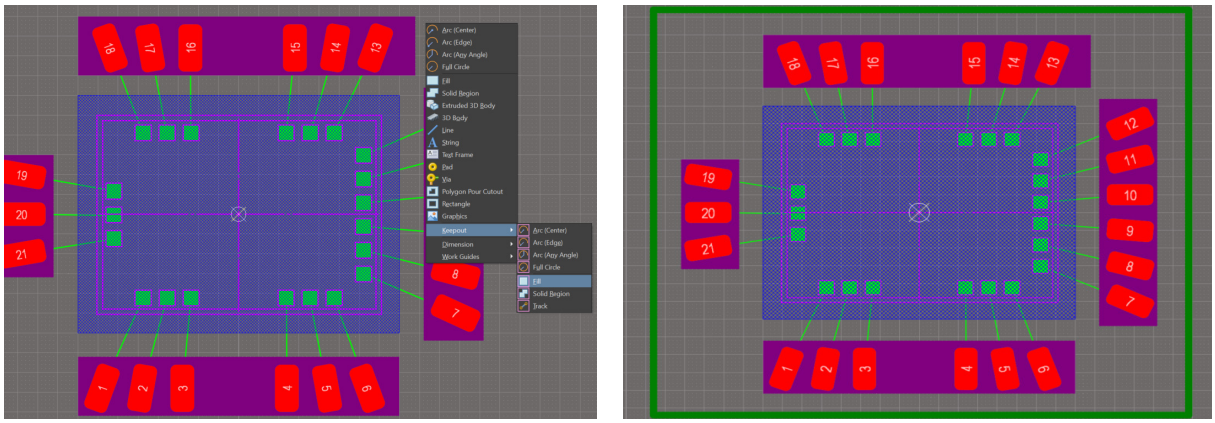


Figure 64. Placing keepouts and courtyards

STEP 8: Generating fabrication data

After completing the routing of your design, the primitives that we created in the “Wire Bonding” mechanical layer now need to be exported and included in the fabrication output files. If Gerber files are required, then the wire bonding mechanical layer needs to be selected in the list of layers in the Gerber setup window.

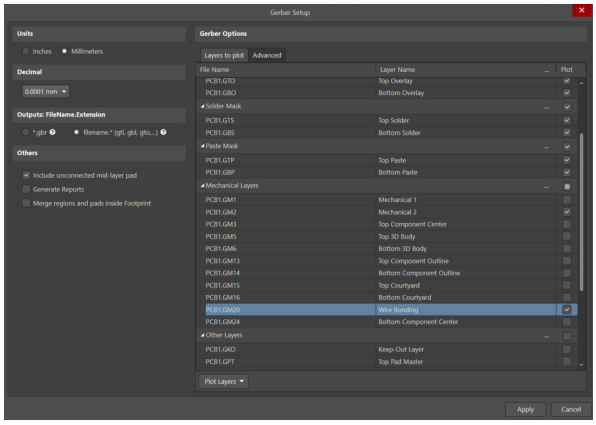


Figure 65. Generating fabrication data

Once the Gerber files have been generated, Altium's CAM editor can be used to verify and check the wire bonding data.

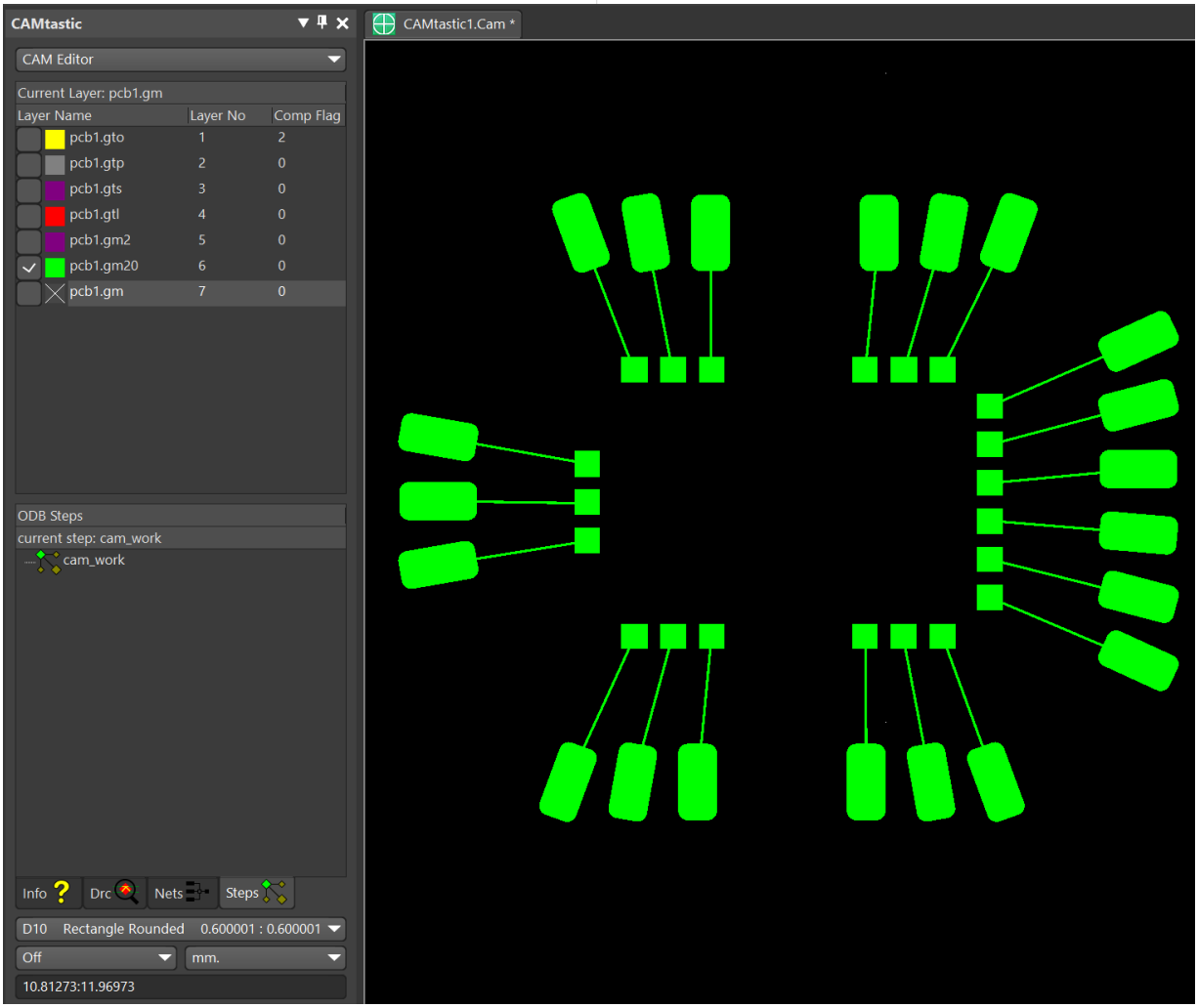


Figure 66. Viewing wire bonding data in the CAM editor

We have now completed our COB with wire bonding design.

Comparison

The new Wire Bonding capability in Altium Designer (AD2x) provides users with capability to create COB designs with accurate representation and modeling of wire bonds. This new feature makes die creation and wire bond specification an integrated part of the design. Altium Designer now has a dedicated layer pair for bare die, and die pads can now be assigned to Nets and classes which then can be controlled with Design Constraints.

Previous methods of representing COB design with wire bonds relied on creating mechanical layers and using line primitives to represent wire bonds or adding dedicated wire bonding signal emulating layers inside layer stacks. These methods did not accurately represent the die and wire bonds and perhaps were suitable for low complexity and simple designs, but with today's high density and advanced designs, the dedicated Wire Bonding feature in Altium Designer AD24X is certainly well suited to address these challenges.

The table below highlights the new features and capabilities of Altium Designer's integrated Wire Bonding feature in AD2x compared to the previous methods of representing wire bonds.

	Wire bonding feature (post AD2x)	Without wire bonding feature (pre AD2x)
Wire bond & die pad net assignment	Yes	No
Wire Bond 3D visibility	Yes	No
Wire bond geometry specification (diameter, bond type, loop height)	Yes	No
Pad Actions - alignment & orientation	Yes	Needs to be done manually
Constraints and Design rules checks	Supported	Not supported
Query language	Supported	Not supported
Draftsman support	Supported	Not supported
Wire Bonding Output Reports	Yes	No

8. Conclusions

Wire bonding technology, which first came about after the invention of the transistor, has continuously evolved to meet the higher performance demands, greater power density, and more compact designs in today's electronics industry. It provides reliable and cost-effective interconnections essential for Chip-on-Board (COB) applications, enhancing and enabling new advanced design concepts such as 3D integrated circuits and stacked die. Wire bonding ensures high-density interconnections supporting high-resolution image sensors, and compact, high-performance LED arrays. It is also essential for unlocking the full potential of wide-bandgap semiconductors such SiC GaN helping achieve higher efficiency and power density in power electronics.

Wire bonding integration with PCB design tools like Altium Designer allows for accurate modeling, optimizing placement, and improving performance, driving innovation in modern electronics. Wire bonding is a reliable technology with well-understood failure modes, addressing mechanical, electrical, thermal, and environmental challenges. It will continue to be pivotal in developing advanced, reliable, and efficient electronic systems.

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