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Signal Analyzer by Keysight

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ALTIUM DESIGNER25

by KEYSIGHT

Demystifying Signal Integrity

Introduction

Signal integrity is all around us. Take verbal communication, for example; there is a speaker (transmitter) and a listener (receiver). If anything happens to the sound signal going from the speaker to the listener, the listener will not understand the speaker's message, just like a signal integrity (SI) problem. This principle applies to digital communication systems as well.

In today's fast-paced design environment, the increasing demand for higher data rates and smaller printed circuit boards (PCBs) makes signal integrity a critical consideration for every designer. Without taking care of the channel between the digital transmitter and receiver, even the most advanced systems can suffer from data corruption or outright failure.

This guide explains the essentials of Signal Integrity (SI), offering PCB designers an overview of common SI problems and the tools needed to analyze designs effectively.

Define Signal Integrity in Digital Communication

As engineers design PCBs to transfer more data per second from the transmitter to the receiver, the system's signal integrity becomes increasingly important. But what is Signal Integrity?

Signal integrity refers to the problems interconnects introduce and how to avoid them [1]. Figure 1 shows the digital communication path from the central processing unit (CPU) to a display monitor.

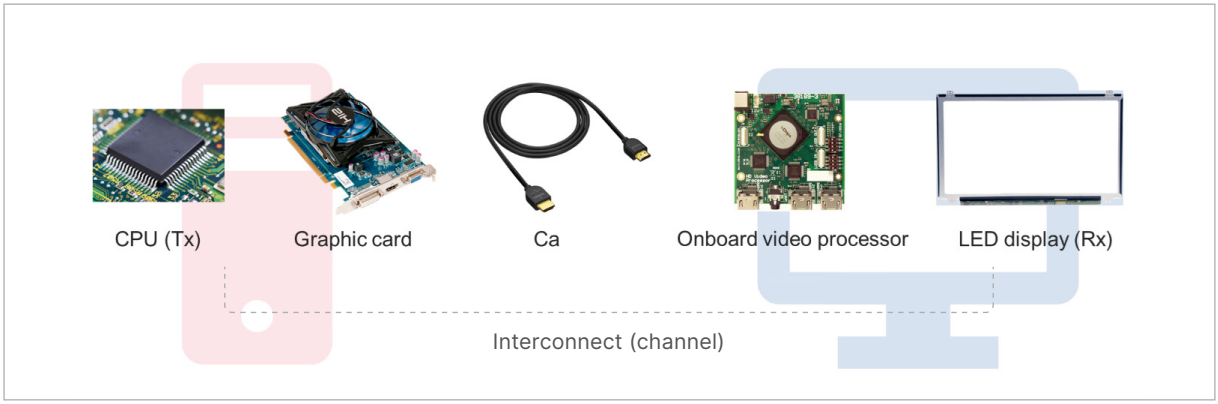

Figure 1. Demonstration of a digital communication channel.
The components between the transmitter and receiver are called the interconnect.

The CPU acts as a transmitter, the Tx, and the display is a receiver, the Rx. The interconnect refers to all the intermediate connecting components from the Tx to the Rx.

As the signal travels through the interconnect, also known as the channel, the quality of the signal will degrade, and signal integrity is the study of what causes these changes and how to improve them.

Understand the Signal Integrity (SI) Metric

Metrics are the backbone of signal integrity analysis, helping designers measure performance and identify potential design problems. The eye diagram is one critical metric for understanding SI.

The eye diagram provides a system-level view of the interconnect's signal integrity and visually shows the engineer how the channel degrades the digital signal. Figure 2 shows examples of two eye diagrams at a receiver. An open eye indicates good signal integrity, where a digital one and zero can be distinguished at the receiver. A closed eye indicates poor signal integrity, where the receiver cannot tell whether a one or zero is received.

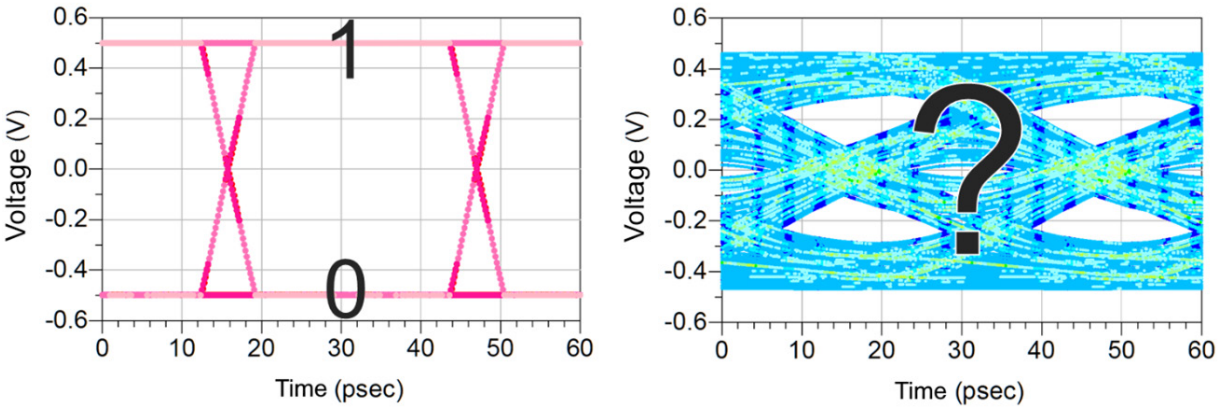

Figure 2. Left: an open eye in an eye diagram. The eye is open because a digital one or zero can be easily distinguished. Right: a closed eye in an eye diagram. The eye is closed because one cannot distinguish one from a zero.

Eye Diagram Construction

An eye diagram is constructed by processing many transmitted binary sequences. One sends a Pseudo-Random Binary Sequence (PRBS) from the transmitter to the receiver to mimic user digital data traveling through the interconnect. The random nature of the sequence ensures that different combinations of 1s and 0s are sent.

Figure 3 shows an example of PRBS running at the data rate of 10 Gbps (Gigabit per second). The data rate of the PRBS pattern conveys how fast data is transmitted. The inverse of the data rate is the unit interval (UI), which is the time duration of each bit. For a 10 Gbps data transfer rate, the time duration for each bit is 0.1 ns. In other words, a 10 Gbps signal has a 0.1 ns unit interval (UI).

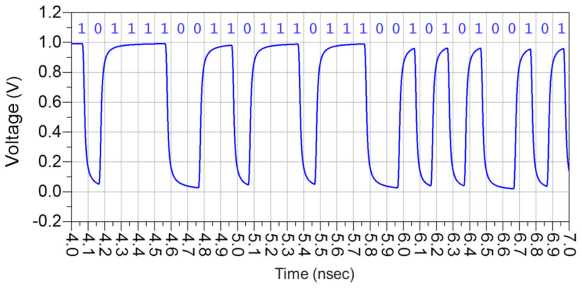

Figure 3. A 10 Gbps Pseudo-Random Binary Sequence (PRBS) sent from the transmitter to the receiver.

As shown in Figure 4, the PRBS pattern can be partitioned at every two unit-intervals. These partitions are stacked on each other to create the eye diagram we see.

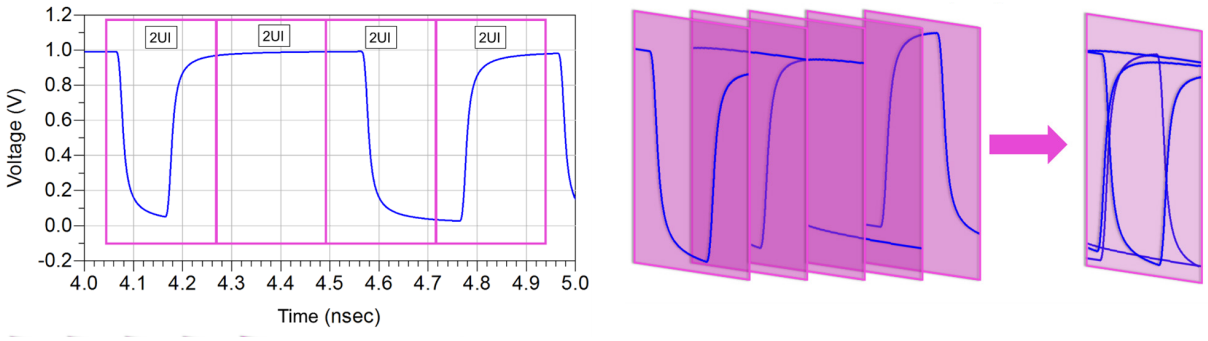

Figure 4. Top: demonstration of two-unit-interval partitions on a PRBS pattern.
The eye is created after partitioning the binary sequence by every two-unit interval and stacking the partitions.

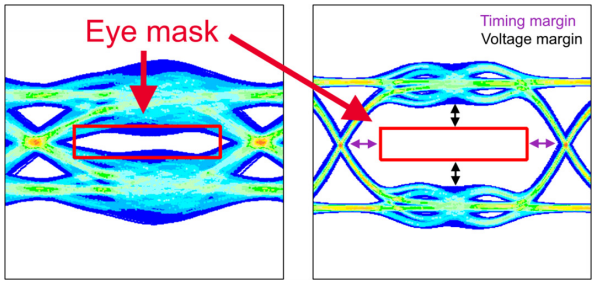

Figure 5. Left: an example of a bad eye, where the eye diagram overlaps the eye mask. Right: an example of a good eye where the eye diagram and eye mask are far apart from each other.

Examine the Eye with Eye Masks

Eye masks are often used as keep-out regions to define the eye's goodness clearly. The vertical voltage threshold and the horizontal timing threshold define an eye mask.

A good eye should have a non-overlapping eye mask and eye diagram. The voltage and timing distance from the eye mask are the voltage and timing margins. Figure 5 demonstrates how an eye mask helps determine the goodness of an eye diagram quickly.

The eye mask represents the receiver's voltage sensitivity and timing tolerance to distinguish between a digital one and a zero at a given data rate. If the eye diagram clears the eye mask with no overlaps, the receiver can differentiate a digital one from a digital zero.

Common SI Problems and Their Signatures

Understanding common signal integrity problems – reflection, crosstalk, and frequency-dependent loss – helps PCB designers avoid pitfalls that can compromise performance. By studying the signatures of the common signal integrity problems, designers can easily identify the root causes and fix them.

Reflection

Reflections occur when transmitted signals encounter impedance discontinuity. At the interface of the two different impedances, part of the signal will be reflected, and part will be transmitted. The reflected signal will travel back toward the transmitter and can be reflected to the receiver. This leads to eye height distortion in the eye height and reduced signal quality; see Figure 6.

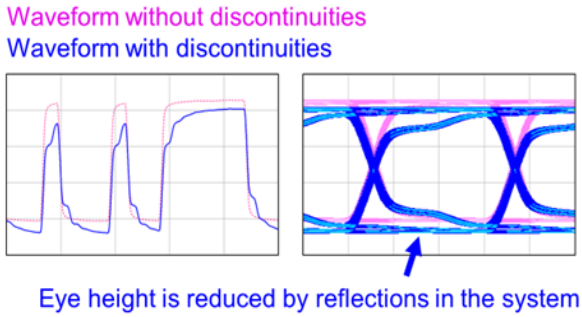

Figure 6. Demonstration of the impact of reflections on the received waveform and eye diagram.

Fix: Ensure the traces are designed with controlled impedance throughout the signal path. Appropriate termination at the transmitter and receiver is also important.

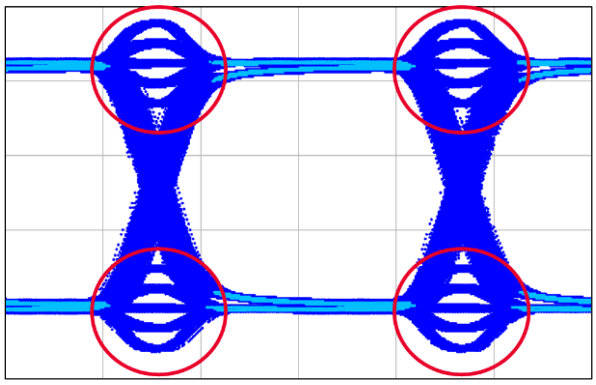

Figure 7. Typical crosstalk signature in the receiver eye looks like peaking in the transitions.

Crosstalk

Crosstalk arises when the traces are close, and the electromagnetic coupling between adjacent traces becomes significant.

In an eye diagram, a typical crosstalk signature in the receiver eye looks like peaking in the transitions (from zero to one or from one to zero), see Figure 7.

Fix: Increase the spacing between traces and route traces as stripline.

Frequency-dependent Loss

As the transmitted signal travels through the interconnect, the high-frequency components often experience more attenuation due to frequency-dependent conductor and dielectric losses. This frequency-dependent loss causes rise time degradation and reduces the openness of the eye.

As shown in Figure 8, a lossy channel reduces the sharpness of the zero-to-one transition (rise time degradation) because the high-frequency components are attenuated. One also notices a reduction in amplitude after the lossy channel.

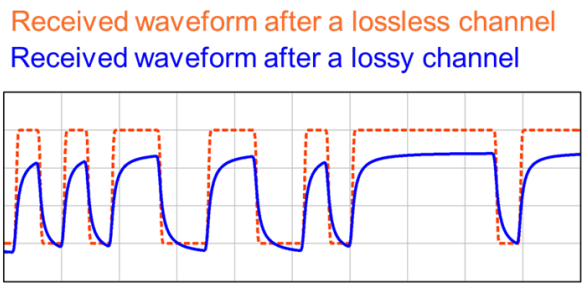

Figure 8. The loss in a channel reduces the amplitude of the signal as well as the rise time.

As shown in Figure 9, the rise time degradation shows up in the transition zone of the eye diagram. Instead of having an extremely fast transition from zero to one, the eye has a slower transition time because the lossy channel attenuated the fast/high-frequency components.

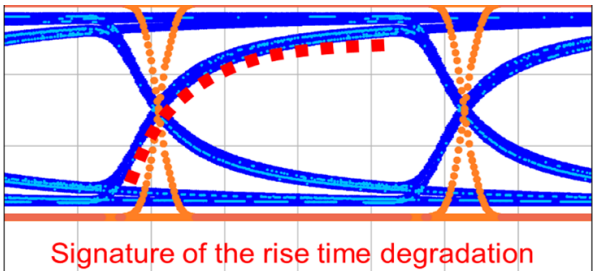

Figure 9. The signature of rise time degradation is shown in the dotted red line. Instead of a fast transition from zero to one, as in the orange eye diagram, the blue eye diagram's transitions take longer because of the frequency-dependent loss.

> **Fix:** reduce trace length and use low-loss dielectric

Analyze SI in the 21st Century

Advancements in electronic design automation (EDA) tools and simulation technology and now provide PCB designers with powerful capabilities for analyzing and optimizing signal integrity. Selecting the right tools involves focusing on three critical attributes:

- Industry Reputation and Validation
- Integration with Your Design Workflow
- Software Usability and Visualization

Industry Reputation and Validation

Look for EDA tools with a proven track record in the industry. Signal integrity software, which is widely used and recommended by professionals, often offers reliable and well-tested features, minimizing risks in critical designs.

Integration with Your Design Workflow

Signal integrity analysis should fit into your existing design processes. Integrating SI software into your current PCB design and analysis workflow can save you time and reduce errors.

Usability and Flexibility

Signal integrity analysis software must be powerful, accessible, and adaptable to different workflows. Effective software provides intuitive interfaces that streamline complex analysis, making it easier for designers to interpret and act on results.

Conclusion

Signal integrity is more than an optional consideration in modern PCB design; it is an essential foundation for high-speed and high-performance systems. The increasing demands for higher data rates mean that designers must prioritize understanding and addressing SI issues before they appear.

Having leaned the construction of eye diagrams and the different signatures of common issues such as reflections, crosstalk, and frequency-dependent loss, you now have a comprehensive understanding of SI and its impact.

By understanding SI analysis and integrating it into the design process, engineers can ensure robust and reliable PCB designs that meet the demands of modern technology.

Signal Analyzer by Keysight - New Solution for Signal Analysis in Altium Designer

Introduction

Signal Analyzer by Keysight in Altium Designer was created to help designers address Signal Integrity challenges directly within their design environment, eliminating the need for external tools or extensive expertise. This guide will walk you through how to use Signal Analyzer by Keysight for comprehensive signal integrity analysis, including impedance matching, delay optimization, and insertion/return loss evaluation. With its intuitive interface, advanced heatmap visualizations, and powerful reporting capabilities, Signal Analyzer by Keysight streamlines the design process and empowers engineers to confidently tackle signal integrity challenges, ensuring first-pass success for high-speed PCB designs.

Using The Keysight Signal Analyzer Extension in Altium Designer

Installing Signal Analyzer by Keysight

To access the Signal Analyzer by Keysight functionality in Altium Designer, the Signal Analyzer by Keysight extension must be installed. The extension is located on the Purchased tab of the Extensions and Updates page, which can be accessed by selecting the Extensions and Updates command from the user menu at the top right of the design space.

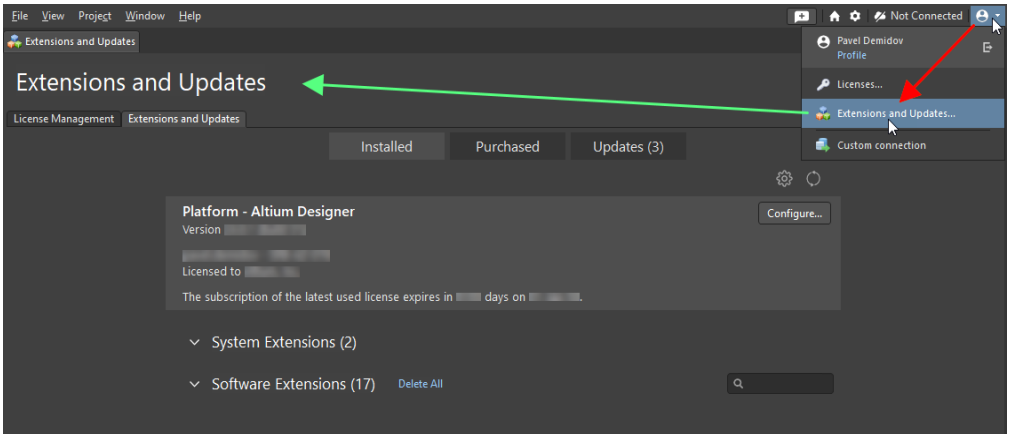

Figure 10. Accessing Extensions & Updates

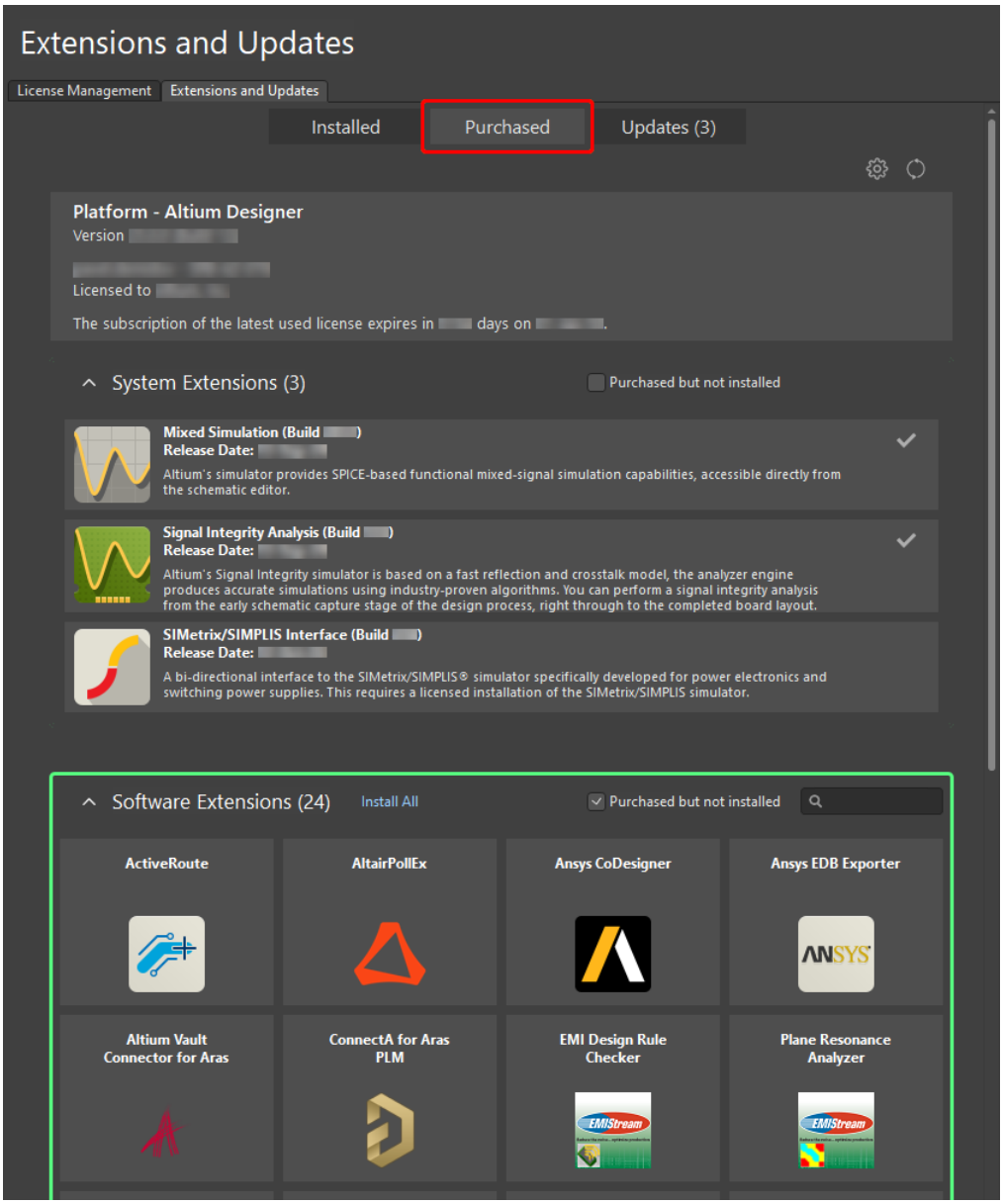

Figure 11. Where to Download the Signal Analyzer by Keysight Extension

Power & Signal Analyzer Bundle from Keysight Read Article

To install the extension, hover the cursor of the extension icon and click the download icon that appears.

When you click to download and install the extension, the End-User License Agreement will open. You will need to press accept to complete the installation. Once installed you'll need to activate your license.

Figure 12. Signal Analyzer by Keysight Extension

Getting a License

To get a license navigate to the Licenses section which can be found in the user menu at the top right of the work area. When you open in the License Management section will display a list of available licenses for your account. If purchased, you should see a license for Signal Analyzer by Keysight. Click on the “Use License” Button next to the license line item to activate it.

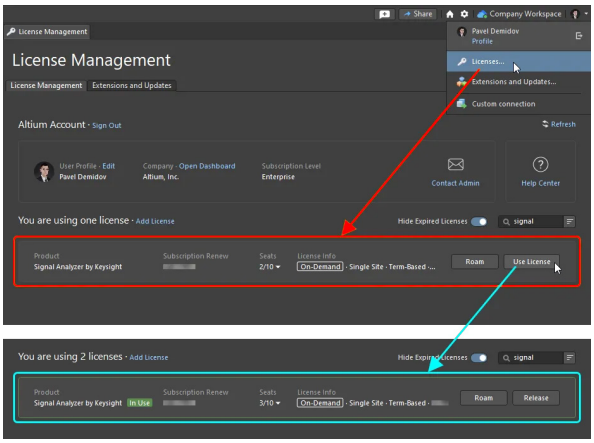

Figure 13. How to Access License Management

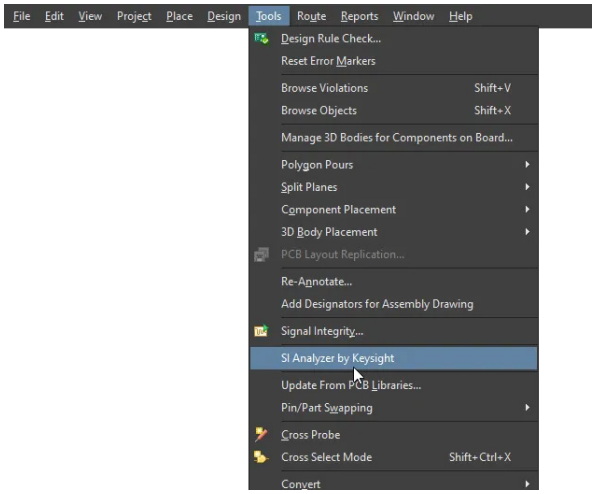

Figure 14. How to Open Signal Analyzer by Keysight

Launching Signal Analyzer by Keysight

To start signal integrity analysis, open the project’s PCB document and select Tools » SI Analyzer by Keysight from the main menus.

Selecting and Setting Up Nets and Analysis

After launching Signal Analyzer by Keysight, the PCB data is imported (in the ODB++ format) to the solver. At this stage, you can define the list of nets to be analyzed and assign specifications to them.

To do this, click the Manage Nets button at the top of the Signal Analyzer document or use the Edit » Manage Nets command from the main menus.

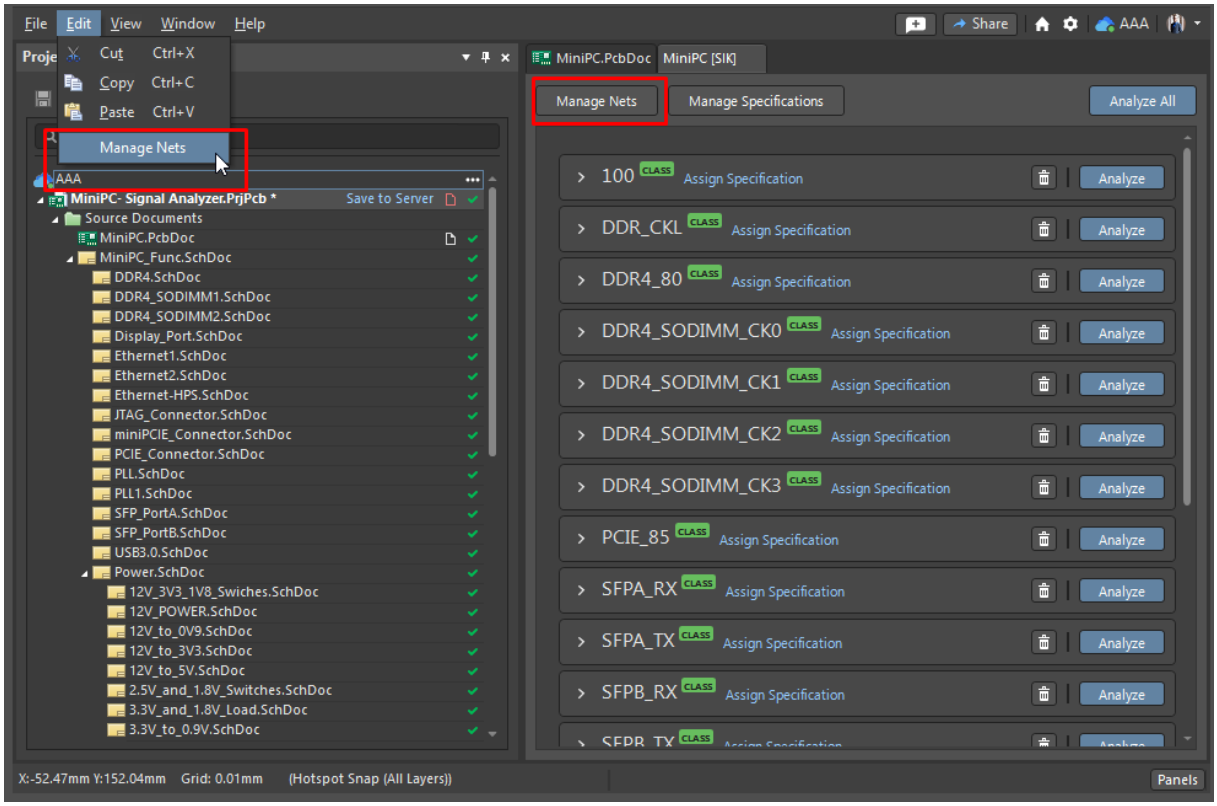

Figure 15. Select Manage Nets to Add Nets to Analyze

If there are no nets in the document, the Manage Nets button is also available in the center of the document. The Manage Nets dialog opens, presenting the list of the PCB's net, differential pair and xSignal classes.

It is important to note that Differential pair and xSignal classes of the PCB design are initially added to the document automatically when it is created. Also, if a class does not contain objects, it will not be available for selection in the Manage Nets dialog.

The Manage Nets popup dialog is where you can add and remove nets to be included in your analysis. You can search by name or by scrolling through the options.

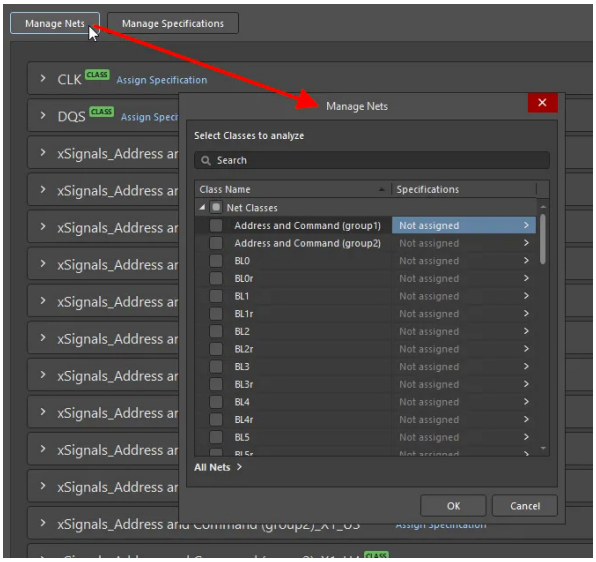

Figure 16. Select Net Classes & Nets from the Manage Nets Popup

Specifications for each Net or Net Class can also be assigned within the Manage Nets popup. These specifications can be predetermined or customized for each net.

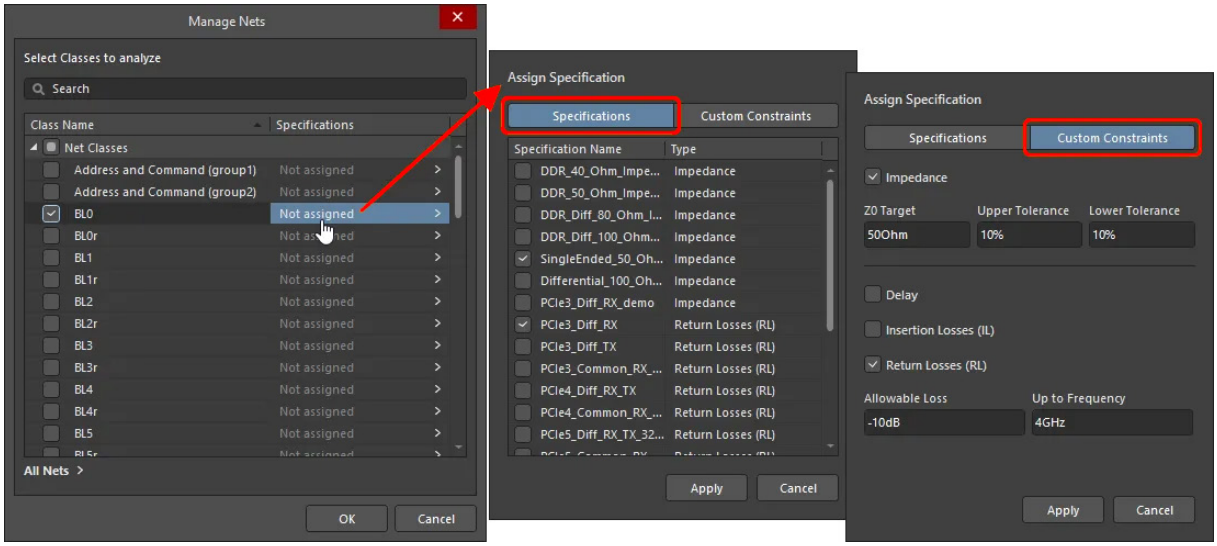

Figure 17. Applying Analysis Constraints

Although you can specify net constraints during the net selection process. This can also be done afterwards.

After clicking OK on the Manage Nets popup, the selected net and net classes will be shown in the main window. You can also assign specifications for each net and net class here by clicking on “Assign Specification”, next to each entry.

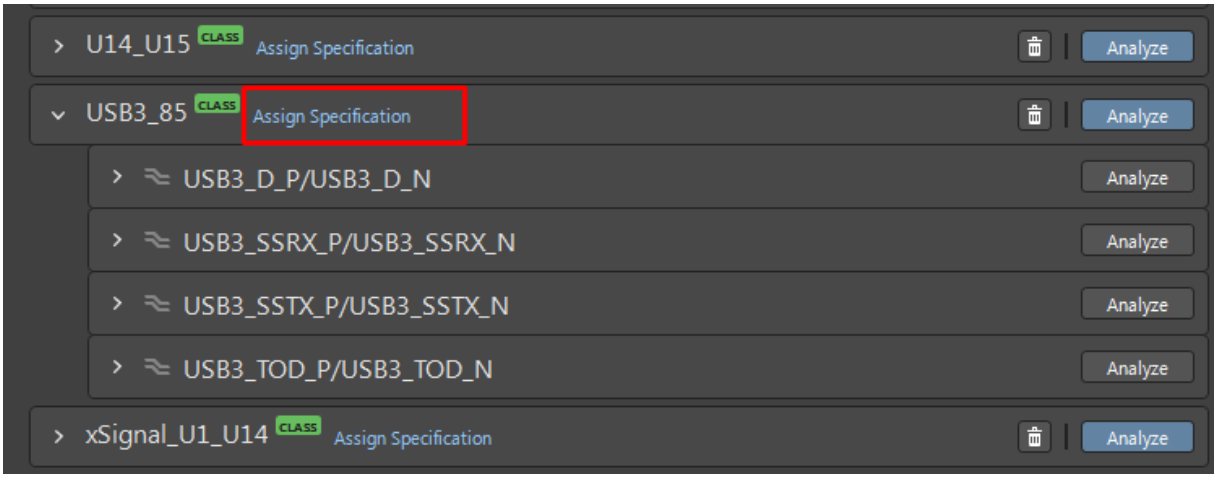

Figure 18. Select Assign Specification to Apply Analysis Constraints

The Assign Specification window will appear. You can select predefined constraints or create your own.

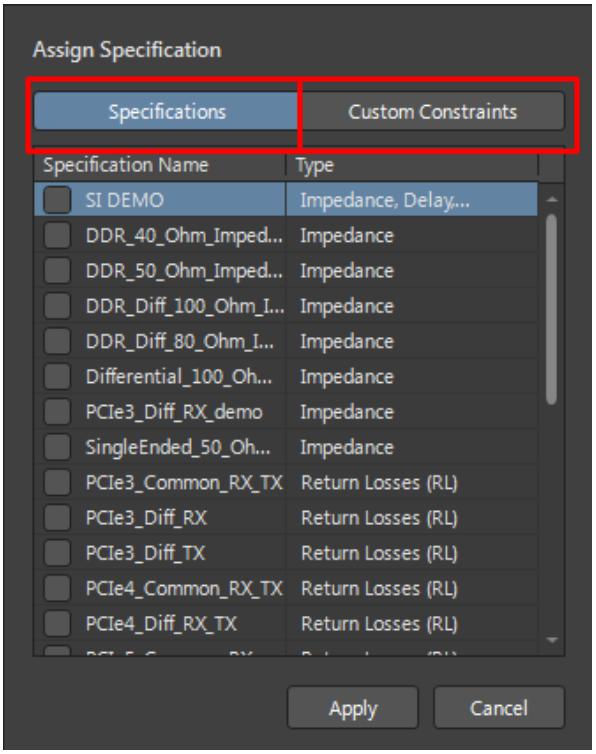

Figure 19. Select a Predefined Constraint or Create Your Own Custom Constraints

You can create custom constraints for Impedance, Delay, Insertion Losses, and Return Losses. Just select which constraints you would like to customize and input your values.

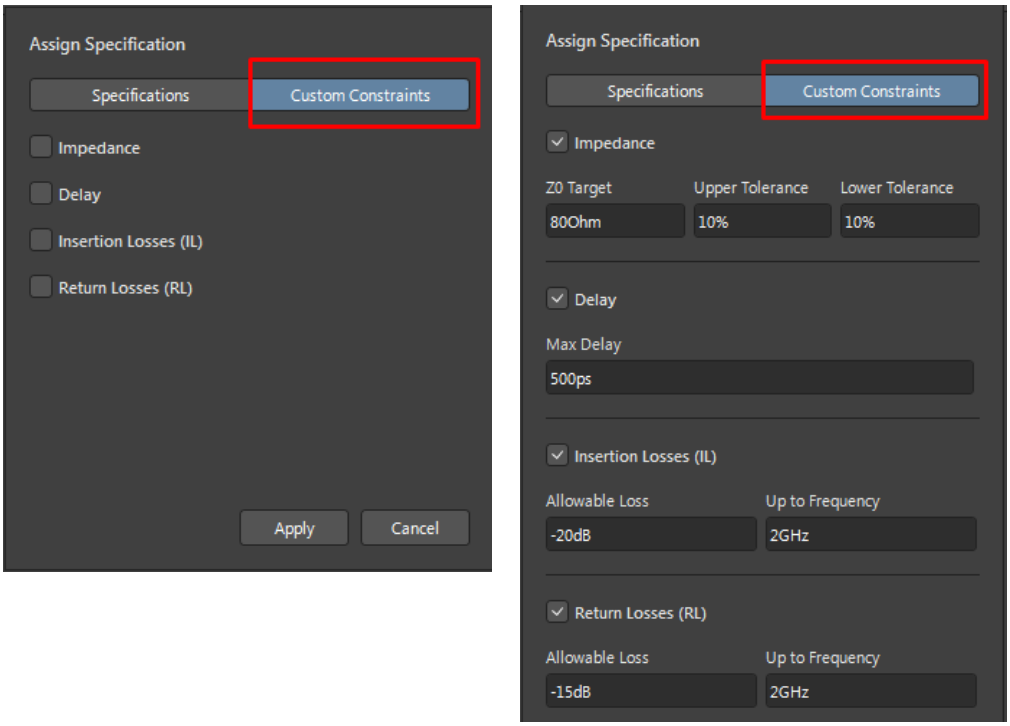

Figure 20. Select Your Constraints and Input Your Values

After setting up your nets and constraints your workspace should look something like this:

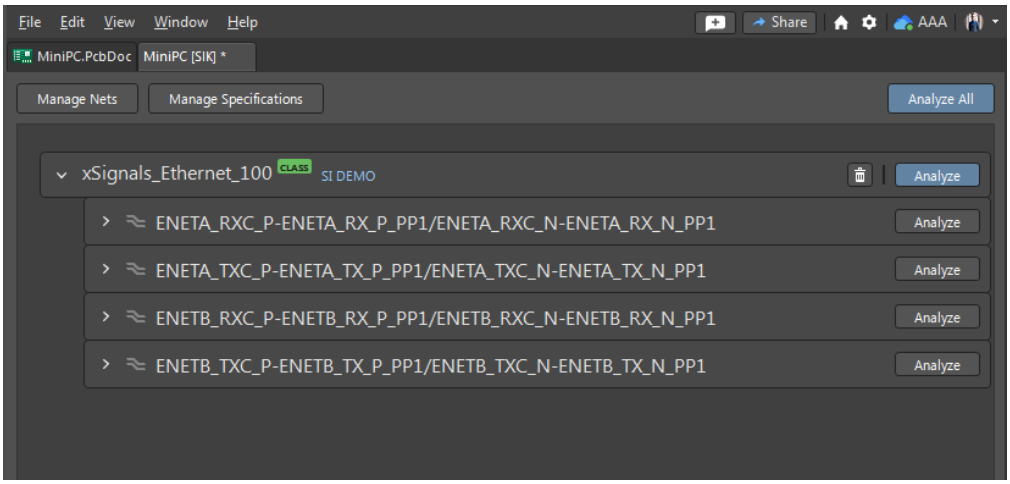

Figure 21. Net Class After Constraints Have Been Set

By expanding the net class, you expose the individual nets. By expanding the individual nets, you expose the transmission line. Next to each net you can show the results (if available) as well as the current constraints.

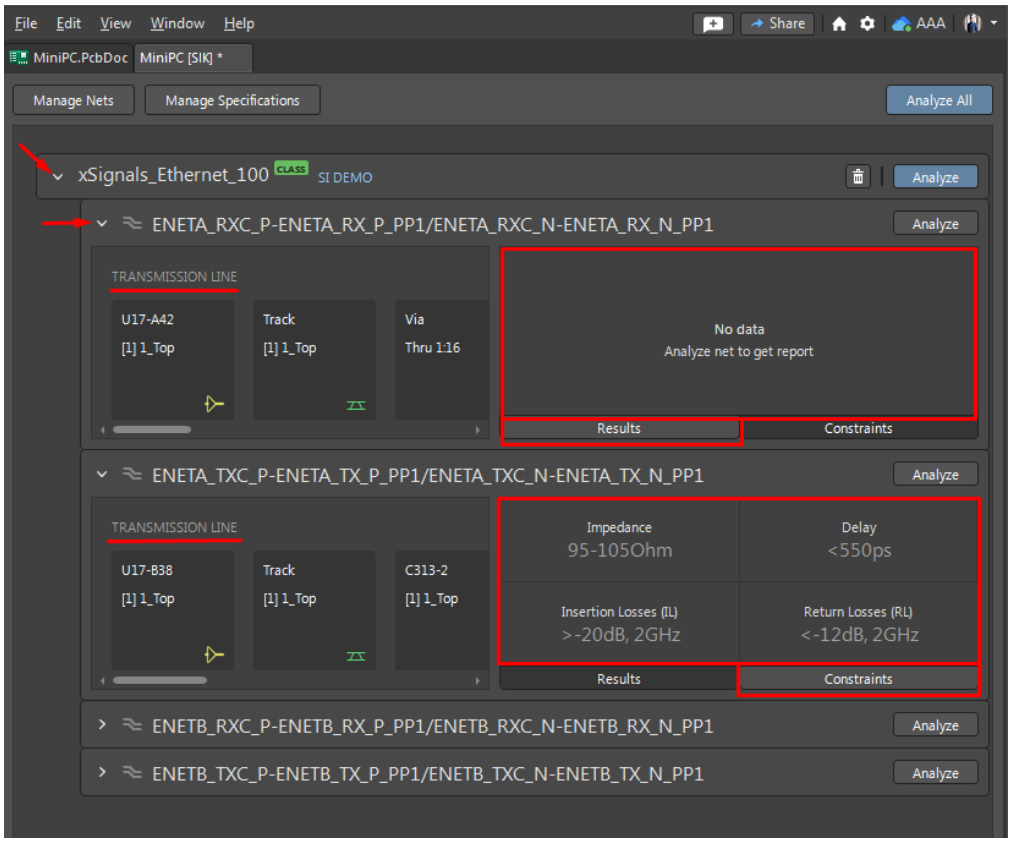

Figure 22. Anatomy of a Net Class Entry

Once all your nets and constraints have been set up you can select “Analyze All” at the top of the page to analyze all the nets or you can select “Analyze” next to each individual net or net class to analyze that specific item.

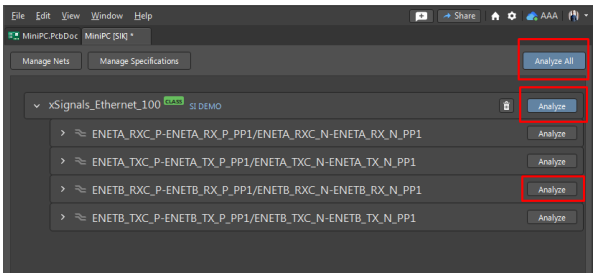

Figure 23. How to analyze your Nets and Net Classes

Once you select the “Analyze” button, the analysis will begin and Signal Analyzer by Keysight will analyze your design.

Understanding Signal Analyzer by Keysight Results

In Signal Analyzer by Keysight

Once the analysis is finished, its results are presented in the Signal Analyzer by Keysight document. The Analyzed message will be shown at the top-right of the document. If all analyzed nets are within the constraints, the All Passed text will be shown next to the message. Otherwise, the Failed text will be shown, with the number of the nets that do not pass your constraints.

Figure 24. Results of the Analysis

If all nets in a class pass the analysis, the “Success” text will be shown for its entry. Otherwise, the Failed text will be shown.

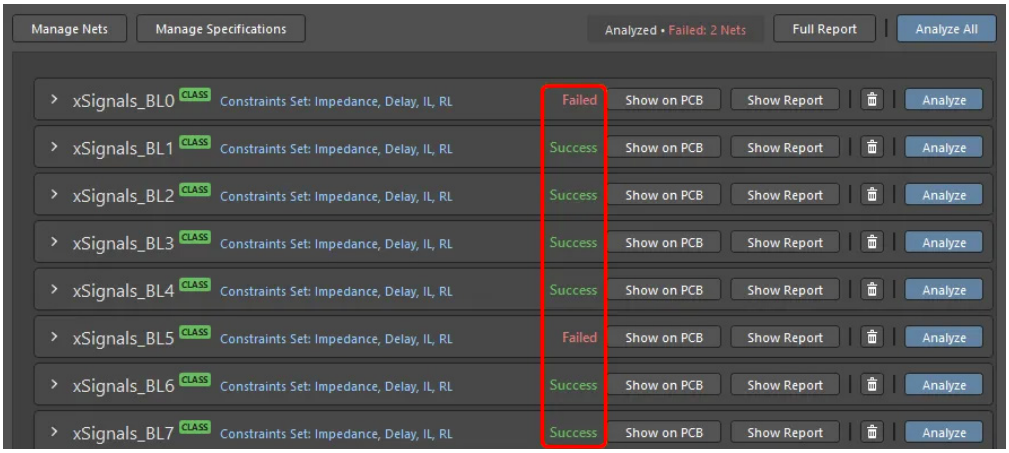

Figure 25. Results are Displayed Next to Each Net Class

Expand a class entry to see the calculated values (impedance, delay, insertion losses, and return losses) for each analyzed net in that class. Values that meet the constraints are shown in green; values that do not meet the constraints are shown in red.

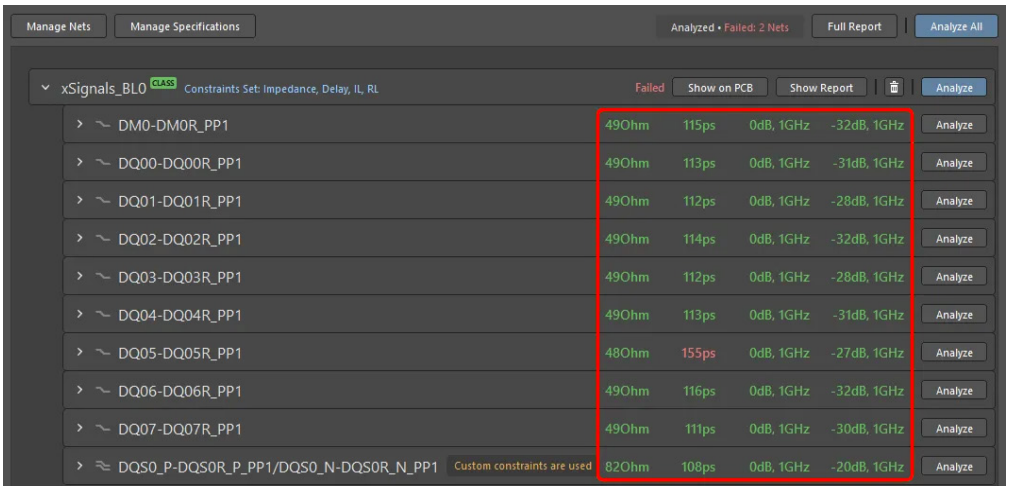

Figure 26. Color Coded Results Displayed for Each Net in a Net Class

Expand a net entry to see the calculated values for this net on the Results tab. Also, tiles of net objects that do not meet the constraints have a red border in the Transmission Line region, and the failed value is shown in red.

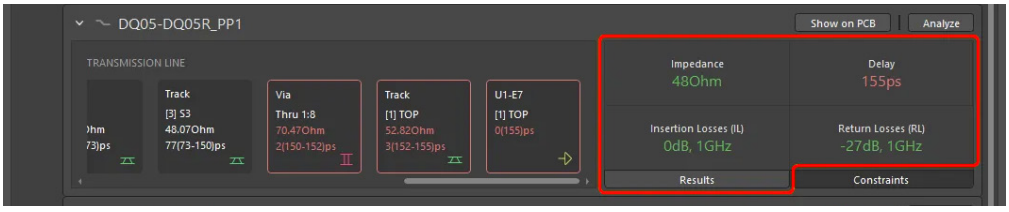

Figure 27. Results of an Expanded Net Within a Net Class

In The PCB Layout

To see the analysis results on the PCB click on the Show on PCB Button next to each Net Class or net.

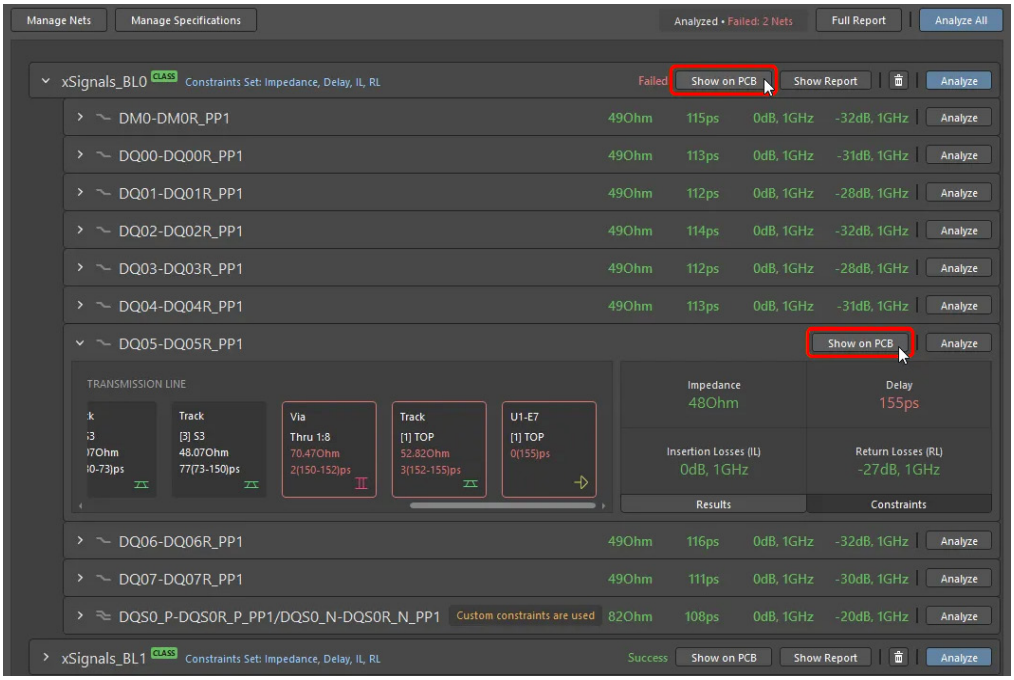

Figure 28. Show Results on the PCB by Clicking on Show on PCB

Doing so will bring up the PCB Layout document and the Signal Analyzer by Keysight panel. If the panel doesn't open, open it from the Panels menu at the bottom right of the window.

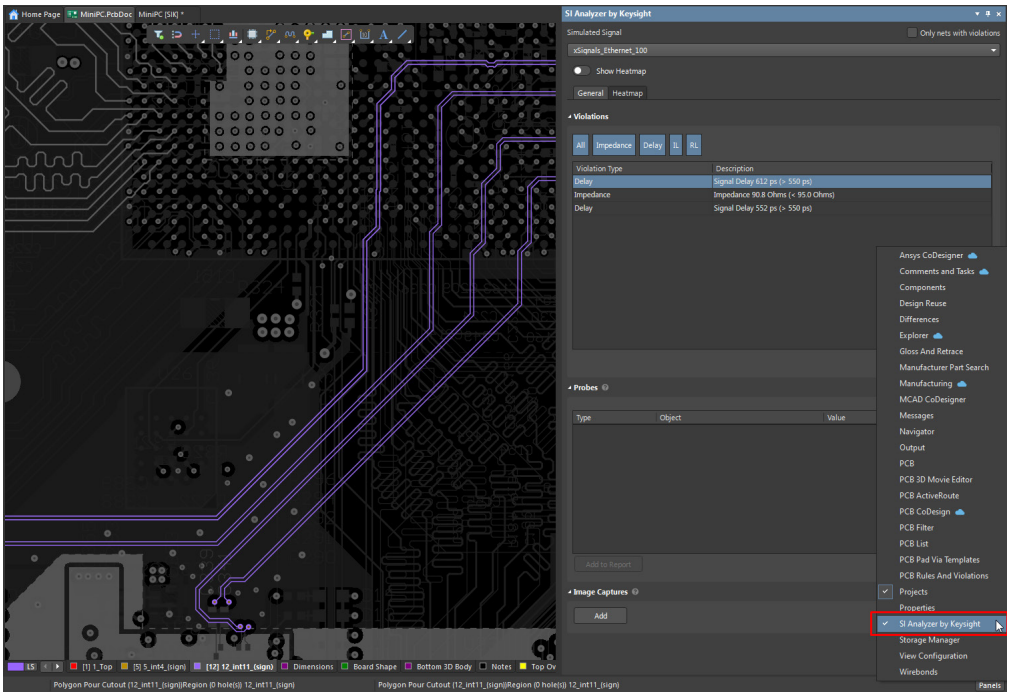

Figure 29. Where to Find the Signal Analyzer by Keysight Panel

Signal Analyzer by Keysight Panel

When working with results in the PCB layout document, the Signal Analyzer by Keysight panel is where you control what and how you display your analysis results.

Let's start at the top, looking at the "Simulated Signal Section". Using the pulldown you're able to select the net class or net you want to work with.

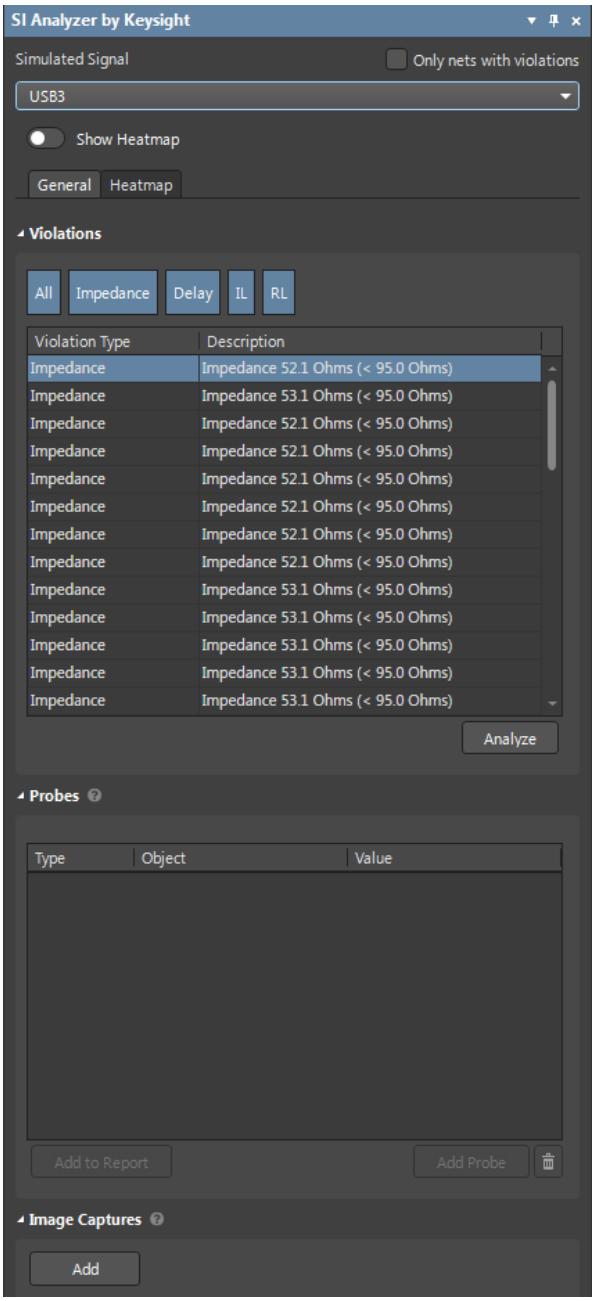

Figure 30. The Signal Analyzer by Keysight Panel

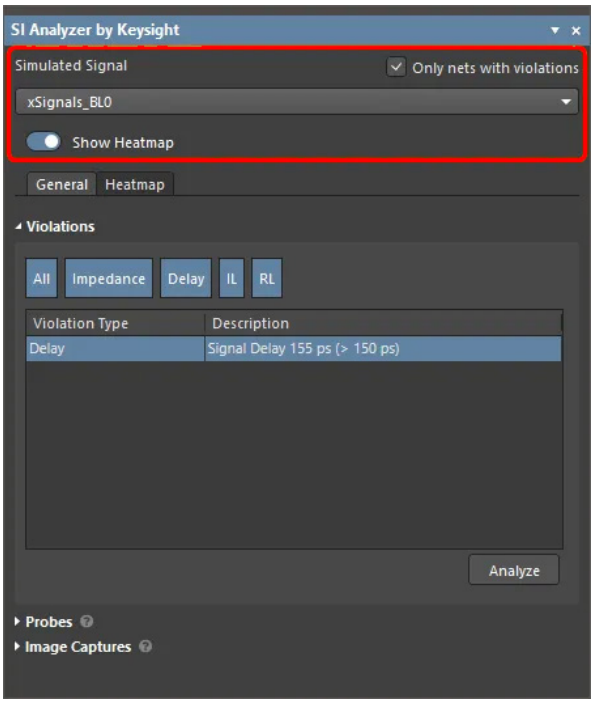

Figure 31. Choose the Signal to Analyze with the Simulated Signal Pulldown Menu

You'll also notice that you can choose to view only nets with violations. This will only show nets with violations in the pulldown menu. This helps to narrow things down and quickly find design issues, especially when you're dealing with a lot of nets.

You also have the possibility of turning on and off the heatmap overlay for the selected net in the PCB environment.

Below these controls, you'll notice the panel has two tabs, General and Heatmap. The options in these tabs apply to the entity currently selected in the Simulated Signal drop-down.

Heatmap Tab

The Heatmap tab is used to control what information is presented as a heatmap, either the impedance or delay. In this section you can also control how color is applied to the heatmap by adjusting your tolerance limits.

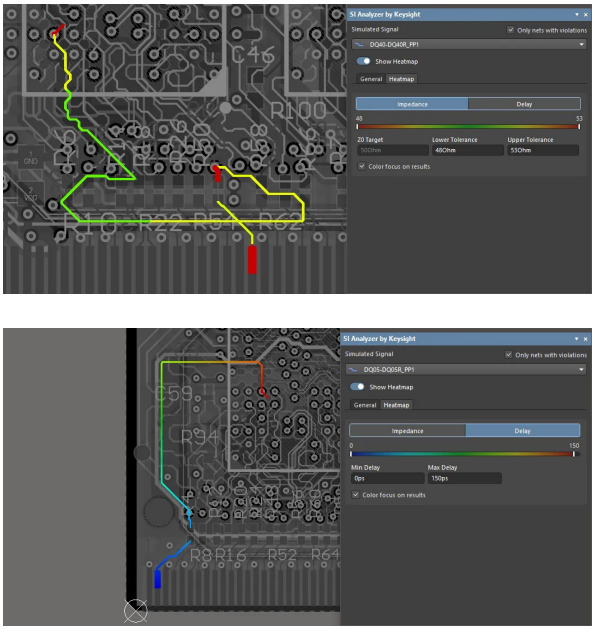

Figure 32. Select Impedance or Delay to Display the Needed Heatmap

You're able to switch between looking at impedance or delay simply by clicking on the "Impedance" or "Delay" button. Here's a quick tip for analyzing the heatmap:

Impedance: The closer you are to your target impedance Z0, the greener your heatmap will be.

Delay: The larger the delay, the redder your heatmap will be.

General Tab:

Looking at the General tab we see three sections: Violations, Probes, and Image Captures.

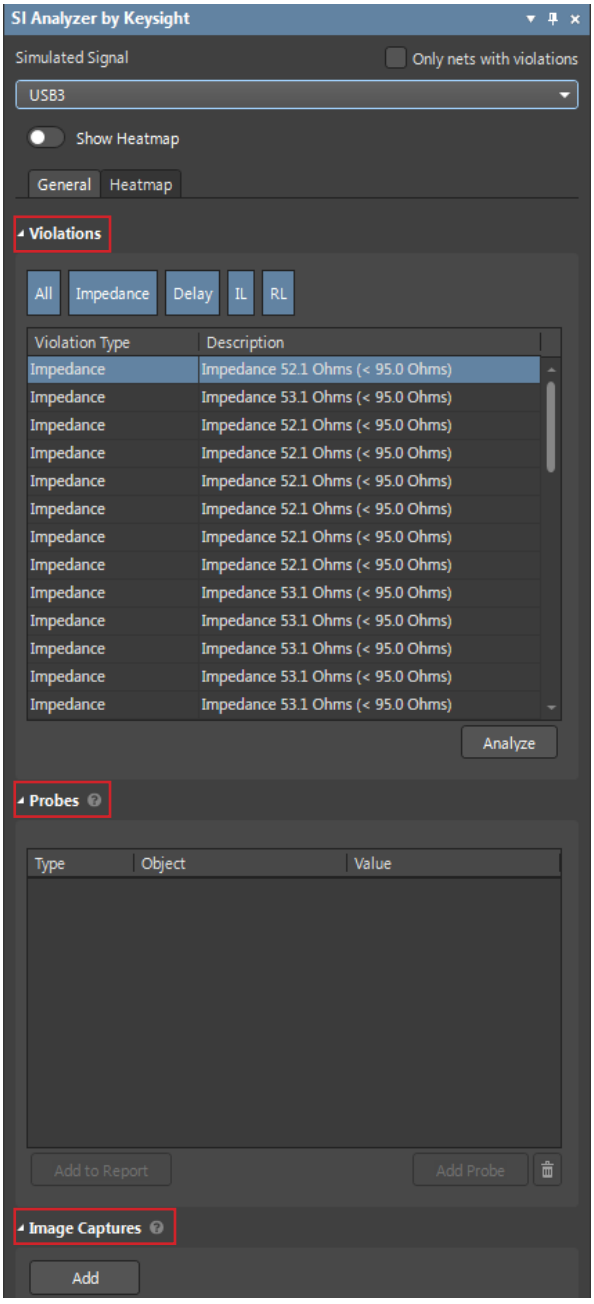

Figure 33. Sections of the Signal Analyzer by Keysight Panel

Violations:

Here you can view all violations of the net or net class you have selected at the top of the Signal Analyzer by Keysight panel under “simulated signal”. Just like the properties panel in the PCB or Schematic, you can filter your violations by clicking on and off the violation types at the top of the violations section of the panel.

Probes:

The probes section is where you can manage the different probe values you’ve captured from your heatmap. Probes can either be a single probe, to measure an absolute value at the probe site, or a difference probe, to measure the difference between the two probe sites. Both types of probes are placed by clicking the Add button in the Probes region of the panel. If the button is greyed out, be sure to turn on the heatmap.

To place a Single Probe, click at the desired location on the heatmap and then right-mouse click (or press Esc). To place a Difference Probe, click once to define the first probe site, then click a second time to define the second probe site. Once a probe has been defined, the measurement results will be displayed in the panel.

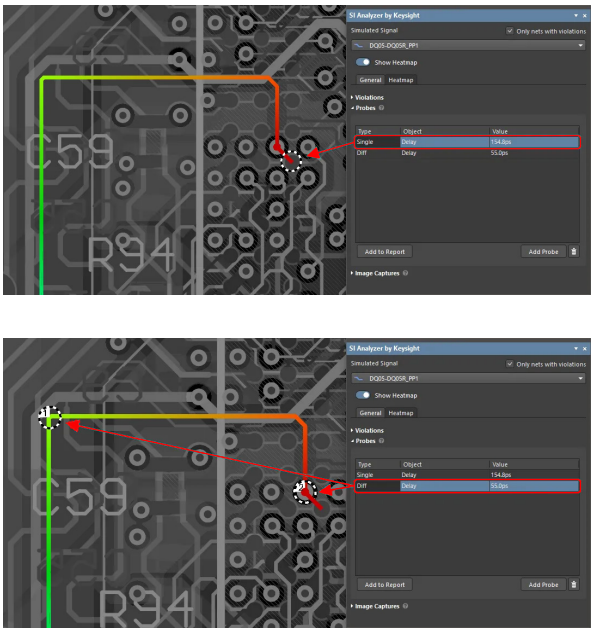

Figure 34. Probes Can Have Single Values or Take the Difference Between Two Values

Once the probe value has been recorded, you can view them at any time by clicking on the probe entry. If you would like to add probe values to a report, click on the “Add to Report” button.

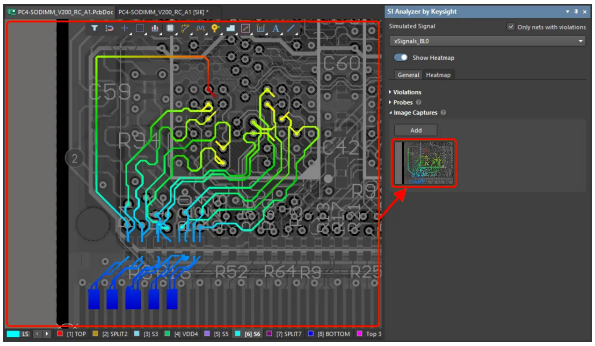

Figure 35. Image Captures Can be Added to the Report

Image Captures

The last section is the Image Captures section, here you can take screenshots of your results which will then be added to your analysis report. Images are saved to the Signal Analyzer by Keysight document, so be sure to save the document to save the images.

To take a picture of a specific area of the board, first, arrange the view of the board in the design space so that the elements you want to be included in the capture are visible. Once ready, click the Add button in the Image Captures region of the panel to capture the screenshot. You can continue to change your view of the board and add more images.

Images can be removed by hovering the mouse over the thumbnail image and clicking on the Trashcan icon.

Report Generation

Incomplete or inefficient documentation can lead to design misunderstandings, compliance issues, and delays in production. Report generation ensures that all signal integrity analyses are clearly documented and easily accessible.

Signal Analyzer by Keysight streamlines this process by automatically compiling detailed reports directly from your PCB layout, allowing designers to share results, confirm design decisions, and meet project requirements with confidence.

To generate a full analysis report, click the “Full Report” button at the top of the Signal Analyzer by Keysight document. The full report includes a section for each class (and the All Nets entry for individually added nets outside of net classes).

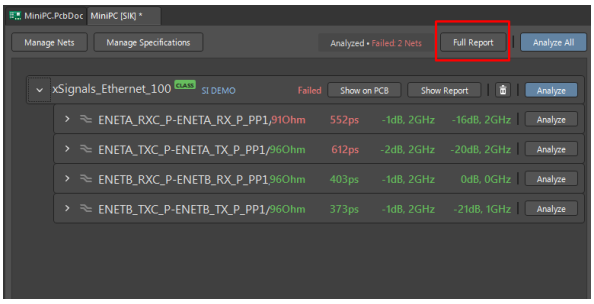

Figure 36. Find Reports by Selecting the Full Report Button

Figure 37. Reports are Created for Each Net Class

Looking at the full report you’ll see a list of net class entries, each representing a separate report. By clicking on the net class name, the report for that net class will open.

Reports will have a several sections:

- Name of the net class or net: Displays the name of the net or net class the report was created for.
- Assigned specifications: Displays the assigned constraints for the net or net class.
- Constraint check summary: by clicking a failed check entry you can see recommendations for how to fix the issue.
- Layer Stackup of the board: displays the layer stackup for the board.
- Constraint checks for each net: You can expand a net entry to see constraint checks for each object of this net.
- Interactive Insertion losses chart: displays insertion loss for each net. Magnitude vs frequency

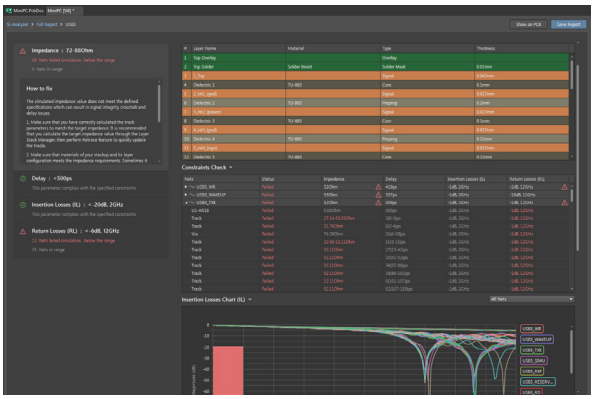

Figure 38. View of a Full Report

Saving a Report

If you would like to save a report, click on the Save Report button at the top of each individual report to save the individual report, or the Save Report button while looking at the full report to save all the reports at once.

A Report Settings popup will appear where you can finger the report before generation. After clicking the Generate Report button, the report will open in your browser. The report is also stored locally in a sub-folder in the project folder named:

\SiAnalyzerByKeysight_Output\HTMLReport\<ProjectName>.sik_<CurrentDate>_<CurrentTime>

All the images in the report are stored in an Images sub-folder.

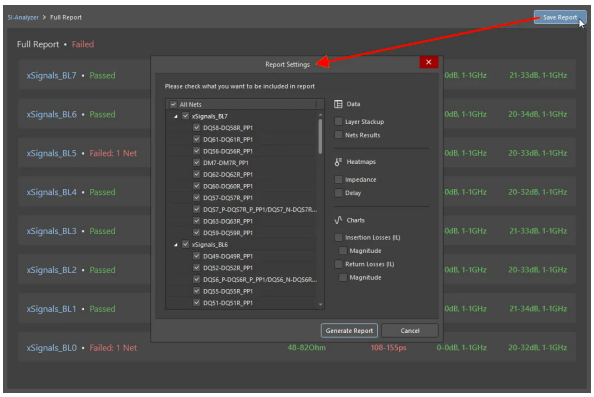

Figure 39. Customize Your Report

Impedance Analysis

Impedance mismatches are a common cause of signal integrity issues, leading to signal reflections, loss of data, and degraded performance in high-speed PCB designs. Signal Analyzer by Keysight makes it easy to identify and resolve these mismatches by providing detailed impedance analysis directly within Altium Designer.

Use Case

A PCB designer working on a high-speed design for a PCIe 4.0 interface notices intermittent data errors during testing. These errors could be due to signal reflections caused by impedance mismatches along the high-speed data lines.

By using Impedance Analysis in Signal Analyzer by Keysight, the designer can:

- Pinpoint where impedance mismatches occur along the trace.
- Quickly find if trace width, spacing, or material stackup needs adjustment.
- Adjust the design in real-time to achieve the target 85 Ω differential impedance, ensuring reliable signal transmission and minimizing costly rework.

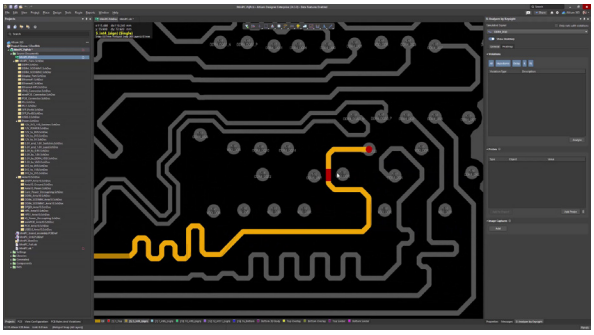

Figure 40. Impedance Analysis

Things To Look For:

- Ensure correct stackup information and dielectric constant (Dk) values are used during analysis to get exact results.
- Watch for discontinuities due to vias, connectors, or sudden changes in trace geometry.
- Impedance changes in manufacturing processes can occur—always verify tolerances with the manufacturer.

Delay Detection

Timing discrepancies in high-speed circuits can cause data errors, synchronization issues, and degraded system performance. Delay detection ensures signals arrive on time by finding timing mismatches across traces. Signal Analyzer by Keysight simplifies this process by providing detailed delay analysis directly on your PCB layout, helping designers adjust trace lengths, keep proper synchronization, and optimize overall design performance.

Use Case

A PCB designer working on a high-speed DDR5 memory interface notices timing discrepancies between the data and clock signals, causing synchronization issues. By using Delay Analysis in Signal Analyzer by Keysight, the designer can:

- Show signal paths with excessive delay.
- Adjust trace lengths to synchronize signal arrival times.
- Ensure best performance by preventing data corruption and timing errors.

Things To Look For:

- Make sure that both clock and data signals have the correct delay margins; overcorrecting can create new mismatches.

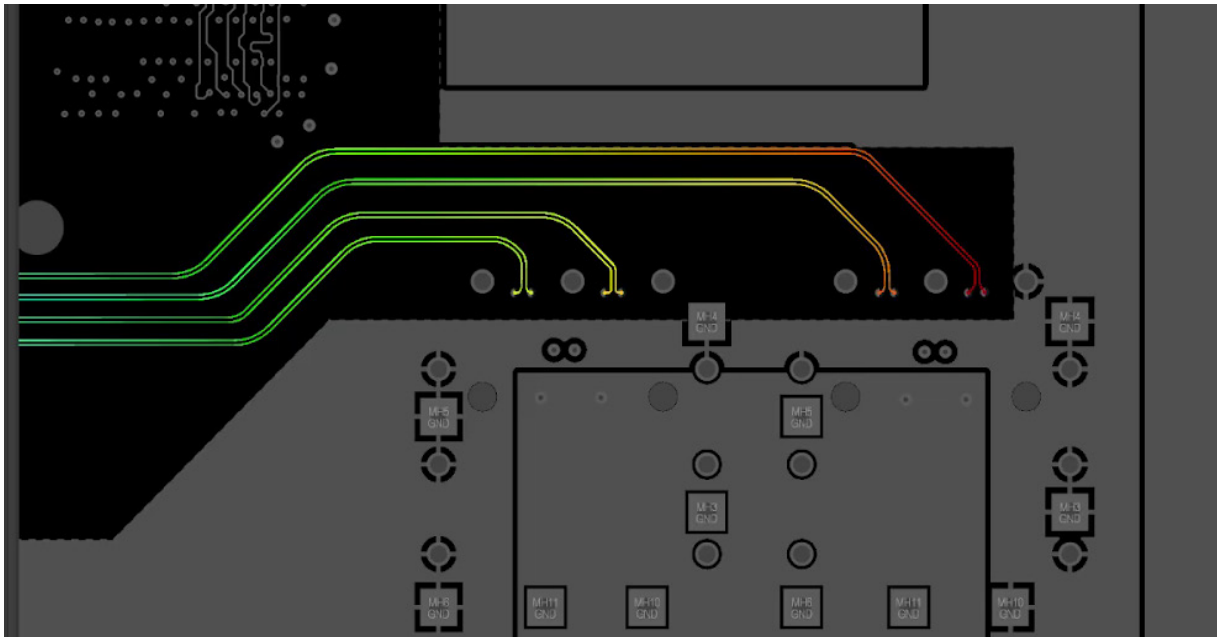

Figure 41. Delay Detection

Insertion loss and return loss are the metrics that inform designers of the amount of loss and reflection in the system. Insertion loss measures how much signal strength is lost along a trace, while return loss indicates signal reflections due to impedance mismatches. Excessive insertion and return loss degrade the total signal integrity of the high-speed signals and might result in system failure.

Signal Analyzer by Keysight simplifies the detection and visualization of both losses directly within Altium Designer, helping designers identify problem areas, improve trace geometry, and improve overall signal transmission efficiency.

Use Case

A PCB designer working on a PCIe 5.0 interface notices performance issues during signal transmission tests, such as data errors and reduced bandwidth. Investigation reveals that long trace lengths and poor impedance matching are contributing to insertion and return loss.

Using Signal Analyzer by Keysight, the designer:

- Quickly finds nets with losses exceeding design parameters using a magnitude response plot, highlighting frequency ranges where signal degradation occurs.
- Adjusts trace impedance, via structures, and connector placements.
- Refines signal transmission, ensuring minimal loss and reliable high-speed performance.

Things To Look For:

- Ensure exact frequency range settings to capture all relevant losses.
- Consider how materials (e.g., copper, dielectric layers) affect insertion loss, especially at higher frequencies.

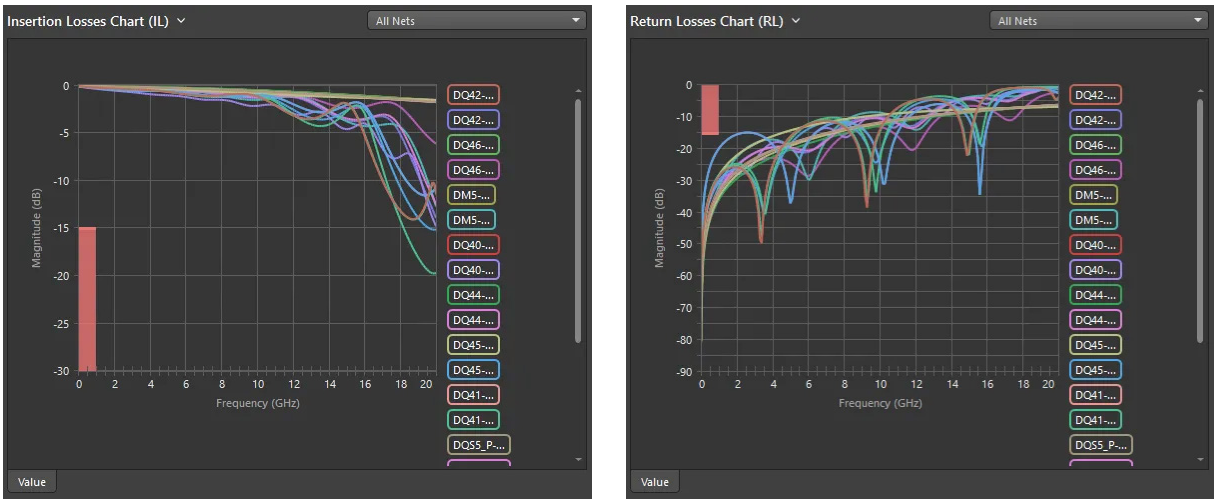

Figure 42. Insertion & Return Loss Charts

Conclusion

As demonstrated, Signal Analyzer by Keysight offers extensive capabilities for Signal Integrity analysis. We invite you to explore our feature page, where you'll find key information about this extension. Additionally, you can install a free trial or purchase the product directly. Visit the link below to learn more:

www.altium.com/products/extensions/signal-analyzer

Reference

[1] Eric Bogatin. Signal and Power Integrity Simplified. Prentice Hall, 2009.